

A TECHNIQUE TO DESKEW DIFFERENTIAL PCB TRACES

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ABSTRACT

A technique for deskewing a pair of terminated, differential PCB traces has been developed in 0.25 μm CMOS technology. The deskewing system utilizes a delay-locked-loop with a digital counter-controlled delay line to match the delay through the positive and negative traces. Time domain reflectometry is used to measure the delay from the terminating resistor to the transmitting chip. The core circuitry occupies 588 $\mu\text{m} \times 235 \mu\text{m}$. Simulation results indicate that skews of over 1 ns can be eliminated using this technique.

1. INTRODUCTION

Many modern high-speed digital systems use differential techniques for high speed signal transmission. Differential signals have several advantages over single-ended signals, such as increased edge rates and greater immunity to noise. To transmit differential signals, two lines are needed - one for the positive signal and one for the negative signal. If the delay through each of the lines is different, then the differential signal at the receiver will be distorted, resulting in a slower data transmission rate for the entire system or potentially causing data transmission errors. The delay between two lines can easily become different in a standard PCB design. Random mismatch between the lines can cause the capacitance or inductance per unit length to be different. In addition, delay differences arise from differences in trace length and loading. If two traces run adjacent to each other, then a turn in the path will cause the total lengths of the lines to be different. Even small differences in the trace delays can cause substantial problems for systems with small timing margins.

The proposed technique will deskew signals transmitted through a pair of differential microstrip lines. In general, when a pair of 50 Ω PCB traces is used to transmit a differential signal to another chip, the traces will be terminated by a 100 Ω resistor at the receiver, as shown in Fig. 1. For a perfect differential signal, the 100 Ω resistor behaves as if it has a virtual ground at its center and provides a 50 Ω matched termination for each line. If the differential signal is distorted due to delay mismatch between the traces, however, the virtual ground will not exist, resulting in unmatched terminations and signal reflections on the lines.

To correct for the difference in delay for a pair of differential lines, an iterative technique is used to add or remove delay to the positive signal path until the skew between the

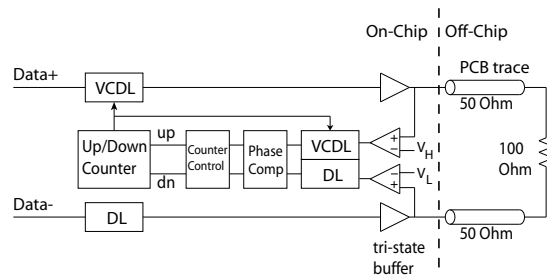


Fig. 1. Proposed Architecture of the Differential Deskewing System

lines has been eliminated. Time domain reflectometry is used to compare the delays through the lines.

2. SYSTEM ARCHITECTURE

Fig. 1 shows a block diagram of the proposed differential deskewing system. A counter controlled digital delay-locked-loop (DLL) is set up around a voltage controlled delay line (VCDL) and the positive PCB trace of the pair. A fixed delay line (DL) in series with the negative PCB trace is used as a fixed delay. On each pulse, the delay through the VCDL and positive PCB trace is adjusted until the delay exactly matches the delay through the fixed delay line and the negative PCB trace and a lock is achieved. For this system, one can calculate the delay from the data inputs, through the delay lines and output buffers, to the receiving chip for the positive (T^+) and negative (T^-) lines. These total delays will be given by:

$$T^+ = T_{vcdl} + T_{buf} + T_{ustrip,p} \quad (1)$$

$$T^- = T_{dl} + T_{buf} + T_{ustrip,n} \quad (2)$$

Where T_{vcdl} is the delay through the VCDL, T_{buf} is the delay of the output drivers, $T_{ustrip,p}$ is the delay through the positive microstrip line, and $T_{ustrip,n}$ is the delay through the negative microstrip line. It has been assumed here that both output drivers are identical and have exactly the same delay. In practice, random mismatch between the drivers will cause the delay through the drivers to be slightly different.

To compare the delays through the PCB traces, the negative output driver is placed into a high-impedance mode and the positive output is pulsed repeatedly using the Data+

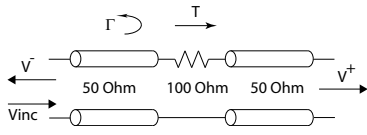


Fig. 2. Circuit Model for a Terminated Pair of Differential Lines

input. Each pulse travels down the positive line and reaches the terminating resistor. At the resistor, the pulse is partially reflected back down the positive line and partially transmitted down the negative line, as shown in Fig. 2. The reflection and transmission coefficients at the end of the line are given by Eq. 3 and 4.

$$\Gamma = \frac{(R_L + Z_o) - Z_o}{(R_L + Z_o) + Z_o} = \frac{1}{2} \quad (3)$$

$$T = 1 + \Gamma = \frac{3}{2} \quad (4)$$

Where Z_o is the trace impedance (ideally 50 Ω) and R_L is the resistance of the terminating resistor (ideally 100 Ω). The magnitudes of the reflected and transmitted pulses are then calculated as shown in Eq. 5 and 6.

$$V^- = \Gamma \times V_{inc} = \frac{1}{2} V_{inc} \quad (5)$$

$$V^+ = T \times V_{inc} \times \frac{Z_o}{R_L + Z_o} = \frac{1}{2} V_{inc} \quad (6)$$

where V_{inc} is the magnitude of the incident pulse. These reflected and transmitted pulses travel back to the chip and are detected on-chip using an appropriately tuned detector on each line. The detectors in this implementation are realized using comparators with one input tied to a DC level[1, 2]. By adjusting the DC level, the detect voltage can easily be adjusted to the correct value. Comparators are used instead of Schmitt triggers in this implementation because comparators exhibit an easily tunable trip point while not sacrificing a fast switching characteristic. The relative phase between the outputs of the two detectors indicates the difference in delays through the two PCB traces. For the system to achieve a lock, however, the delay through each trace plus the delay through the corresponding delay line must be compared. Therefore, the output of each detector is passed through a replica of the corresponding delay line before the relative phase between the signals is compared [3, 4]. The total times required for the signals to travel from the terminating resistor to the phase comparator for the positive ($T_{reflect+}$) and negative ($T_{reflect-}$) lines are given by:

$$T_{reflect+} = T_{ustrip,p} + T_{detect} + T_{vcdl} \quad (7)$$

$$T_{reflect-} = T_{ustrip,n} + T_{detect} + T_{dl} \quad (8)$$

Where T_{detect} is the delay through a detector and it has been assumed that the delays through the detectors for both lines are identical. When the system achieves a lock, $T_{reflect+}$ and $T_{reflect-}$ will be identical. At this point,

$$T_{ustrip,p} + T_{vcdl} = T_{ustrip,n} + T_{dl} \quad (9)$$

When this occurs, $T^+ = T^-$ and the data will be synchronized at the receiver.

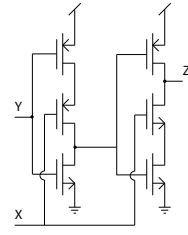


Fig. 3. Precharge-Type Phase Comparator

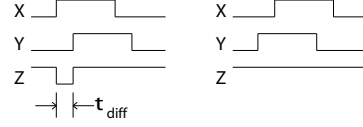


Fig. 4. Phase Comparator Timing Diagram

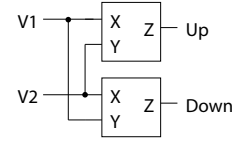


Fig. 5. Phase Comparator Block Diagram

3. CIRCUIT DESCRIPTIONS

The deskew system in Fig. 1 consists of a VCDL, DL, phase comparator (PC), up/down counter, a counter control block to interface the PC to the counter, output drivers, and reflection detectors. The up/down counter and output drivers are built using standard static CMOS techniques. The remaining circuits will be described as follows.

3.1. Phase Comparator

Many conventional phase comparators are limited by a dead zone, where the PC cannot determine the relative phases of its inputs. To overcome this, a precharge-type phase comparator is used [3, 4], as shown in Fig. 3. If the X signal leads the Y signal, then the output will be low until Y rises. Otherwise, the output will remain continuously high. The timing diagram of these events are shown in Fig. 4.

Since the structure in Fig. 3 can only detect if X leads Y, two of these structures are used to create the complete phase comparator [3, 4], as shown in Fig. 5. In this way, the relative phase of the inputs can always be determined.

3.2. Counter Control

The purpose of the counter control block is to allow the PC to interface to the up/down counter. The width of the output of the PC depends on the skew between the PC inputs and becomes arbitrarily small as the inputs become deskewed. The counter clock input, however, requires a minimum pulse width for proper operation. To ensure a minimum pulse width for the counter input the circuit in Fig. 6 is used. A timing diagram of this circuit's output is shown in Fig. 7. In this circuit, an input pulse on the S line

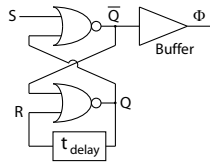


Fig. 6. Counter Control Circuitry

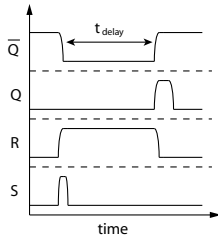


Fig. 7. Counter Control Circuitry

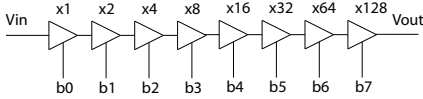


Fig. 8. VCDL Architecture for the Proposed Differential Deskew System

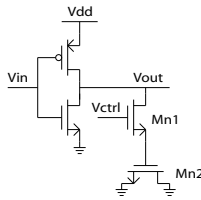


Fig. 9. RC Delay Stage

of arbitrarily small width triggers an output pulse of width equal to t_{delay} .

3.3. Delay Line

Fig. 8 shows the structure of the binary weighted VCDL [5]. The VCDL consists of a number of blocks in series, with each block being tuned to a binary weighted delay as indicated by the multipliers. The number of blocks corresponds to the number of control bits of the VCDL. The maximum delay block is set by the number of bits of the system, N , and will be equal to $t_{min} \times 2^{N-1}$ where t_{min} is the minimum delay increment of the delay line. The maximum delay correction that can be achieved will be given by $t_{min} \times (2^N - 1)$.

The VCDL in this proposal consists of a number of RC-delay blocks in series. The schematic for each block is shown in Fig. 9 [3, 6]. This block is simply an inverter followed by an adjustable load. If V_{ctrl} is high, the gate capacitance from $Mn2$ is added to the signal path. If V_{ctrl} is low, the gate of $Mn2$ is isolated from the rest of the circuit. By placing a large number of these blocks in series, the delay through the entire chain can be controlled.

For the eight-bit system proposed here, the delay is ad-

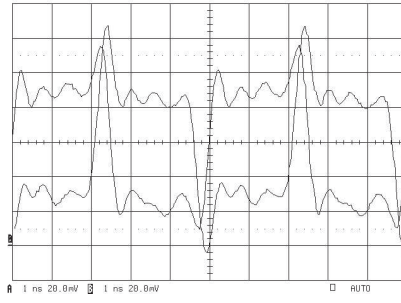


Fig. 10. Waveforms at the Receiver Before Deskewing

justable from 12.5ps to 3.1875ns in increments of 12.5ps. To accomplish this, delay blocks corresponding to 12.5ps, 25ps, 50ps, 100ps, 200ps, 400ps, 800ps, and 1.6ns are built. Delays greater than 50ps are created by placing a number of 50ps blocks in series. This technique helps minimize the effects of broad shifts in process parameters on the relative magnitudes of the delay blocks. In addition, using a larger number of stages with each having a small delay results in smaller duty cycle variations than using a fewer number of stages with each having a large delay.

To ensure monotonicity of delays, the three lowest order bits are coded using a thermometer encoding [7]. In a thermometer encoding, eight 12.5ps blocks are created instead of the three blocks corresponding to the lowest three bits. The appropriate delays for the three bits are created by using the appropriate number of 12.5ps blocks. For example, for a delay of 25ps, the last two blocks are used. For a delay of 75ps, the last 6 blocks are used. Any particular delay is created by taking the next smaller delay and adding an additional 12.5ps block. Since construction of any one delay requires use of the next smaller delay, the monotonicity of delays is ensured.

4. EXPERIMENTAL RESULTS

The system has been fabricated in a TSMC 0.25 μ m, 1P5M process and tested using a 2.5 V power supply. For the test, a custom PCB was fabricated with traces having identical physical dimensions, but a difference in length of 2.1 inches for force a delay at the receiver. In practice, this delay difference can originate from process or load variations between the lines. Waveforms at both terminals of the terminating resistor are shown before (Fig. 10) and after (Fig. 11) correction. As evident in Fig. 10, the delay difference between the traces causes a mismatch in the terminating resistor and ringing on both lines. Deskewing eliminates this ringing, resulting in a much cleaner signal across the terminating resistor, as shown in Fig. 11. The differential signals before and after deskewing are shown in Fig. 12, demonstrating a speedup of approximately 200 ps. A die photo of the chip is shown in Fig. 13. The core circuitry occupies 588 μ m \times 235 μ m.

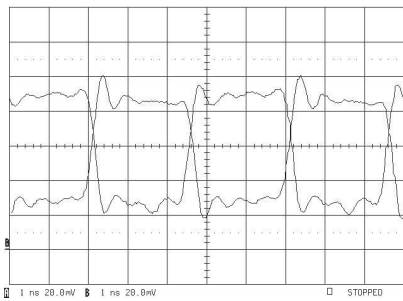


Fig. 11. Waveforms at the Receiver After Deskewing

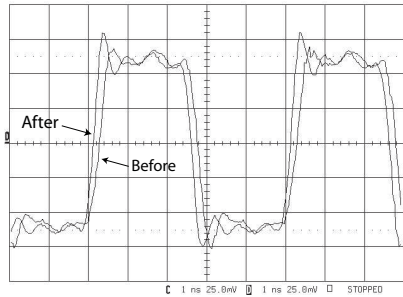


Fig. 12. Differential Waveforms at the Receiver Before and After Deskewing

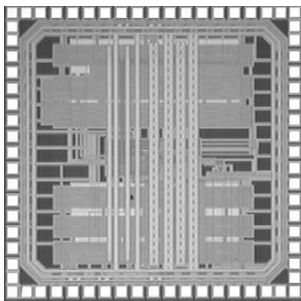


Fig. 13. Die Photo

5. CONCLUSION

In this paper, a technique for deskewing differential PCB traces has been presented. This system implements a DLL using a precharge-type phase detector and a counter-controlled VCDL with a minimum resolution of 12.5ps. The system has been verified through measurement in a $0.25\mu\text{m}$ process and is found to eliminate skews of over 950 ps between traces.

6. REFERENCES

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