Design for MOSIS Educational Program (Research)

A Method to Deskew Differential Microstrip Lines

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Submitted to	**:**	The MOSIS Educational Program (Research)
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Project Description

As process features become ever-smaller, on-chip systems are operating at increasingly higher frequencies. The bottlenecks in system performance are shifting from the characteristics of the devices themselves to the characteristics of interconnects used to connect devices within a single chip and systems built on separate chips. Specifically, one of the problems encountered when attempting to transmit a multi-bit word in parallel between chips is the delay caused by microstrip lines. The length of a microstrip line may vary anywhere from half an inch to ten inches. Differences in length and random variations in the physical characteristics of these lines cause delay variations between any given two lines. When two lines are used to carry a differential signal, this delay difference can degrade the integrity of the signal at the receiver. This project proposes a method to correct for the delay through different-length microstrip lines used for transmission of differential signals such that both polarities of the signal are received simultaneously.

Several techniques currently exist for correcting clock skew within a chip using PLL’s and other voltage controlled delay lines (VCDL). These techniques have primarily been used to correct lines that carry signals referenced to ground. For a single-ended signal, an off-chip microstrip line will be used to carry the signal. This line will typically be terminated with a combination of gate and package parasitic package capacitances at the input of the next chip. When microstrip lines are used to carry differential signals, however, the situation is different. In a previous project, the author developed a technique to correct the delay differences between eight lines of different lengths using time domain reflectometry. In this technique, a pulse was sent down each line when the line is open-circuited at the receiver. The pulse is totally reflected from the open circuit and returns to the transmitter. This reflection is detected at the transmitter using a schmitt trigger. The time between when the pulse is sent on the line and when the reflection is detected is measured and the delay difference between the lines is programmed into a VCDL. This technique was implemented in a chip through MOSIS and experimental results indicate that the chip performed as expected. Delays through eight lines ranging in lengths from 0.5 to 10.5 inches were corrected to within 200ps. The uncorrected delays through these lines ranged from 90ps for the shortest line to 1.8ns for the longest line.

This proposed technique will correct for the delay through a pair of differential microstrip lines. In general, a pair of 50 Ohm differential lines will be terminated by a

100 Ohm resistor at the receiver, as shown in Figure 1. To correct for the difference in delay for a set of differential lines, an iterative technique is used to adjust the delay and time domain reflectometry is used to compare the delays through the lines.

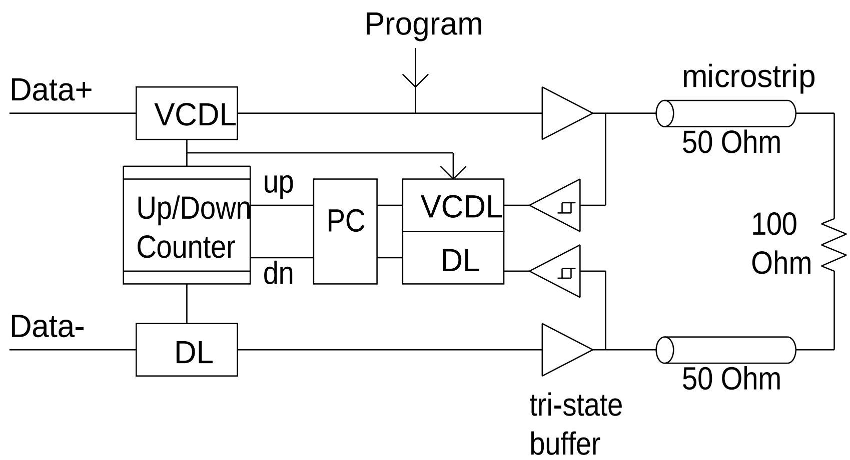

Figure 1. Schematic of the Deskewing System.

In this approach, the negative output is placed into a high-impedance mode and the positive output is pulsed continuously. Each pulse travels down the top line and reaches the terminating resistor. At the resistor, the pulse is partially reflected back down the positive line and partially transmitted down the negative line. These reflected and transmitted pulses are detected using two appropriately tuned detectors. The detectors in this project are implemented as comparators with one input tied to a DC level. By adjusting this level, the detect voltage can easily by adjusted. The relative phases of the detection signals are compared using a phase comparator. The phase comparator controls an up/down counter. The output of the counter feeds into a VCDL that accepts a linearly coded digital control word. In each iteration, the phase comparator either increases or decreases the delay through the VCDL until the phases of the reflected and transmitted waves are identical. If both waves start simultaneously at the resistor in the receiver, then when the waves are synchronized at the phase comparator, the delay line will be programmed such that the Data+ and Data- lines will be synchronized at the receiver.

The VCDL in this proposal consists of a number of RC-delay blocks in series. The schematic for each block is shown in Figure 2. This block is simply an inverter followed by an adjustable load. If Vctrl is high, the gate capacitance from Mn2 is added to the signal path. If Vctrl is low, the gate of Mn2 is isolated from the rest of the circuit. By placing a large number of these blocks in series, the delay through the entire chain can be controlled. For the eight-bit system proposed here, the delay is adjustable from 12.5ps to 3.1875ns in increments of 12.5ps.

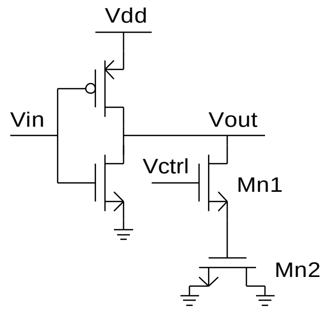

Figure 2. Schematic of an RC Delay Block.

Estimated Project Size

This project will require a total area of approximately $3.25mm^2$ on a TSMC 0.25um fabrication run.

Packaging Requirements

The project will be preferably packaged in an MQFP64A plastic package.

Simulation Plans

The design environment used for this design is Cadence Version 4.4.6. Circuit schematics are simulated using the Spectre simulator within the Analog Artist version 4.4.6 included in the Cadence toolkit. Layout of the circuit is also completed using Cadence (Virtuoso) and the layout is verified using Cadence Diva DRC, extraction, and LVS tools. The Cadence toolkit used for this project is available on the Georgia Institute of Technology network. The TSMC 0.25um library and simulation models were obtained directly from the MOSIS website.

Design functionality was verified through simulations including parasitic capacitances extracted from the layout and estimates for package parasitic inductance and capacitance taken from the package manufacturer's data sheets. Simulations were run at several process corners to help ensure chip functionality.

Test and Characterization Plans

The chip will be tested and characterized using standard test equipment. All test equipment and facilities necessary are available at the Georgia Institute of Technology.