A Universal Sensor Interface Chip with Network Sensor Bus

Final Report to
The MOSIS Service

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Process Details:

Project ID: 68020
Fabrication Process: AMI C5F
Fabrication ID: T37DCC
Design name: umsi3v3
Technology: SCN3ME_SUBM
Die-size: 2.22mmX 2.22mm

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PROJECT DESCRIPTION

A Universal Micro-Sensor Interface (UMSI) has been developed to provide a general purpose, ultra-low noise CMOS IC for the sensor systems. It is intended to support a variety of sensors that require a high resolution of capacitive readout, resistive readout and voltage readouts. The UMSI chip combines a sensor bus interface and the sensor readout electronics to interface a wide range of sensors and actuators to a microsystem controller. It implements a new intra-module sensor bus which is hardware compatible with the standard IEEE P1451.2 TII bus and provides easy deployment, low power, low cost, and high reliability for the microsystem. With the generic analog interface, the UMSI chip can interface with up to 8 capacitive, resistive, and/or voltage output sensors. The circuit level design and the physical layout are mostly completed and it is ready for fabrication. The process used for this design is AMI C5F/N SCN3ME_SUBM.
The bus interface is shown in Fig. 1. It includes shift-in/shift-out, SPI bus interface, interrupt management, memory and controller. The block diagram of the analog front end is shown in Fig. 2. It includes three readout building blocks, a programmable gain stage and a sample-and-hold stage.

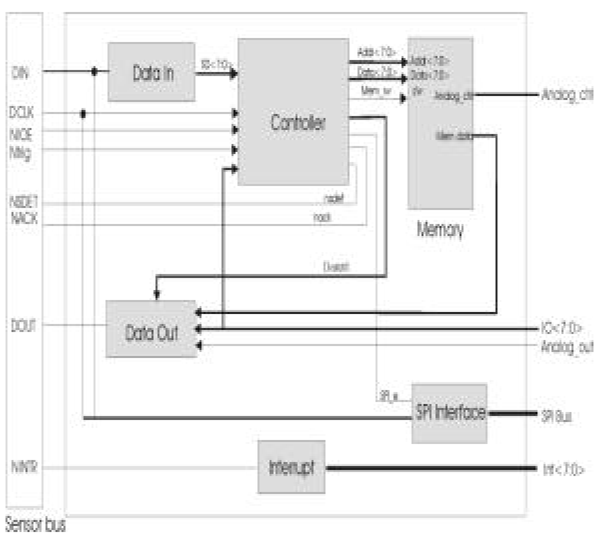

Fig. 1 Block Diagram of Bus interface

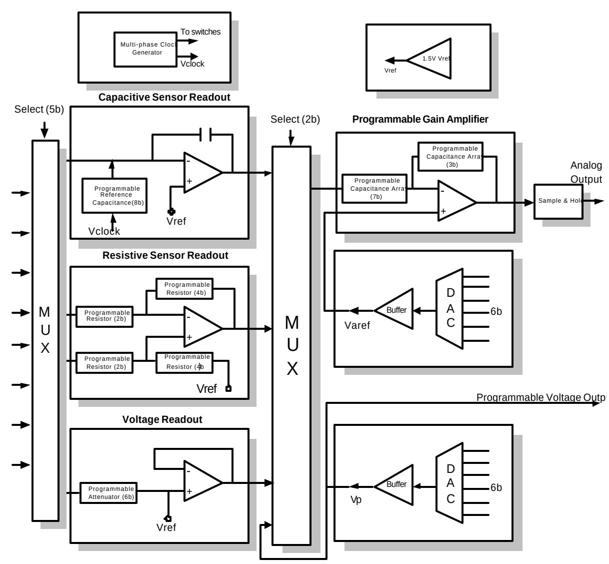

Fig. 2 Block diagram of Analog Core

TEST SETUP

The test setup is shown in Fig. 3. The chip uses separated power supply for digital and analog parts. The supply pin will be connected by a 0.1uF capacitor in parallel. The instruments used for testing include power supplies, a function/arbitrator waveform generator (Agilent 33120A), microcontroller, a mixed signal oscilloscope (Agilent 54622A), a network (gain/phase for amp)/spectrum(noise analysis)/impedance analyzer (Agilent 4395A), and a probe station (Karl Suss) for die testing. The testing items includes read/write memory, chip ID, building block characterization (OTA, reference, DAC), programmable gain SH test, capacitive readout, resistive readout, and voltage readout resolution.

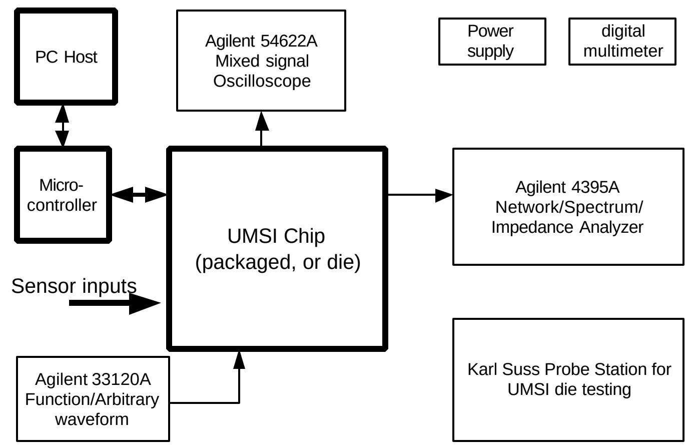

Fig. 3 Test setup for UMSI chip

TEST RESULT OF DIGITAL CORE

The digital part contains a sensor bus, 8bit general I/O and a SPI interface. The sensor bus pins are shown in the Table 1.

Table 1. Sensor bus pins

Pin	Description
NIOE	Signals that data transport is active and delimits data framing
DCLK	Positive-going edge latches data on DIN and DOUT
DIN	Address and data transmitted from MCU to UMSI-III
NACK	Data transport acknowledge
DOUT	Data transmitted from UMSI-III to MCU
NTRIG	Performs triggering function
NINT	Used by UMSI-III to request service from MCU
NSDET	Used by MCU to detect the presence of a UMSI-III

A data transport frame starts when NIOE is pulled low by the microcontroller. The UMSI chip responds by pulling NACK low when it is ready to receive the first chip ID byte of the instruction. If the ID is the same as the assigned UMSI chip ID, the UMSI chip will pull NACK high and continue to receive the subsequent byte. NACK keeps toggling after each byte is received and is finally pulled high when the transport frame is over (NIOE is pulled high by the microcontroller). The function bits specify the operation the interface will perform, such as writing data to the memory, loading ID from IO etc. The timing diagram of the data frame is demonstrated in Fig. 4.

The sensor bus normally works at compact address mode. The number of bytes in one frame depends on the functions. For example, if the function is writing data to memory, the frame will has three bytes. The first byte contains ID and function bits. The second byte is the memory address, and the third is the data. If the function is load ID from IO, there is only one byte in the frame. The NACK will toggle only once.

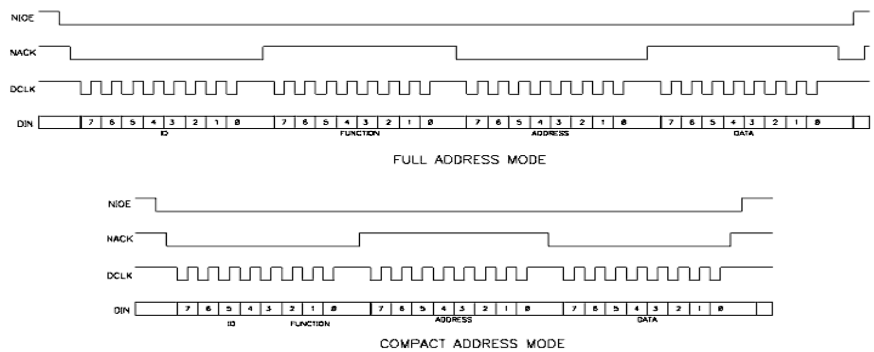

Fig. 4 Timing diagram of writing data to memory.

Assume the sensor bus used compact address mode.

- Connect digital VDD (Pin 16) to the power supply, 3.3V.
- Connect digital GND (Pin 9) to ground.
- Connect the Mode (Pin 14) to ground.
- Set up the chip ID by connecting CID<0:3> (Pin 10-13) to VDD or GND. ID “0” is for broadcasting. So the chip ID should not be set to “0”.
- Keep output pins 15, 18, 29 and 31 float.
- Pin 22-28 is the sensor bus which should be connected to the IO of the microprocessor.
- Interrupt pins and general IO pins are setup depending on the applications.

Note: Pin 32 is also the dout signal of the sensor bus, but it can output analog signal.
Sample test results of writing and reading memory are shown in Figures 5 and 6.

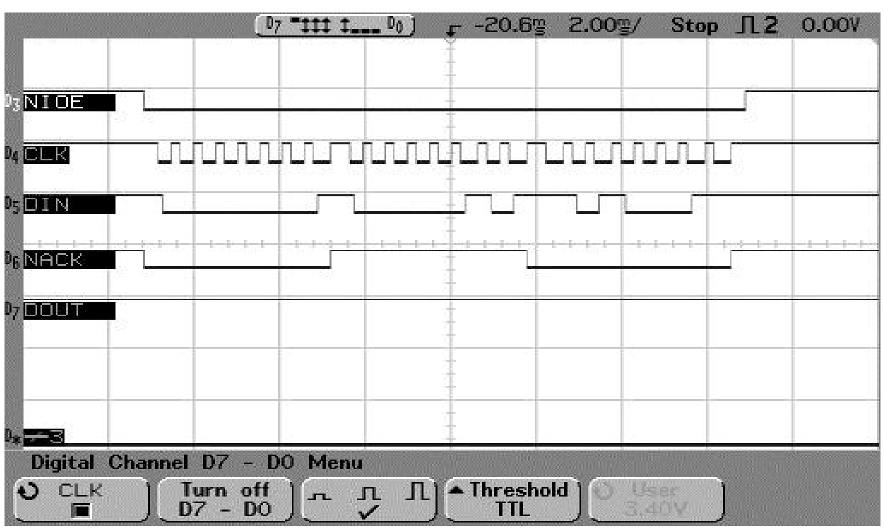

Fig. 5 The microcontroller writes data 0xa3 to memory 5. Frame format: {ID+4’b0001}+{address}+{data}.

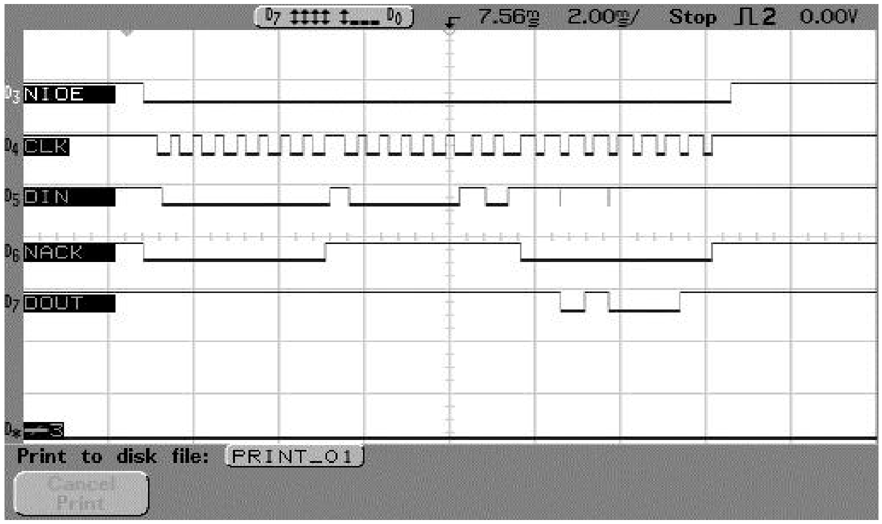

Fig. 6 The microcontroller read data (0xa3) from memory 5. Frame format: {ID+4'b0000}+{addr}+{0}.

TEST RESULTS OF ANALOG CORE

The memory bytes used in programmable analog circuit are listed in Table 2.

Table 2. Memory unit used to control analog interface circuit.

Memory byte	Bit used	Function (used to control the analog part)
Mem 1	6:0	digital inputs for varef DAC
Mem 2	6:0	digital inputs for self test DAC
Mem 13	5:0	8-to-4 signal router
Mem 19	1:0	4-to-1 readout channel selection
Mem 20	2:0	PGA feedback capacitor Cfd (3-bit)
Mem 21	6:0	PGA input capacitor Cin (7-bit)
Mem 23	7:5	Ra (3-bit) control
Mem 23	4:2	Rb (3-bit) control
Mem 23	1:0	Sb_control (bit 1); Sa_control (bit 0)
Mem 24	7:0	Rftuning resistor in on-chip resistive bridge
Mem 26	7:0	Programmable reference capacitor array Cref (8 bit)
Mem 29	1:0	R1 in resistive readout amplifier (7.5 KΩ, 3.75 KΩ)
Mem 29	5:2	R2 in resistive readout amplifier (30KΩ, 15KΩ, 7.5KΩ, 3.75KΩ)
Mem 30	5:0	Programmable attenuator in voltage readout

An 8-to-4 analog signal router allows multiple sensors (or sensor arrays) to access the readout blocks. It is controlled by a 6-bit sensor mode register (mem13<5:0>) on the chip that selects one of the eight inputs and routes it to the proper readout input channel. Table 3 defines sensor mode register data.

Table 3. Functional description of sensor mode register.

Mem13<5:0>	Functional description
$11P_1P_0N_1N_0$	Full bridge resistive sensor readout: positive input is selected by bits P_1P_0 (pins 7-4); negative input is selected by bits N_1N_0 (pins 3-0)
01xx R_1R_0	Half bridge or signal resistive sensor readout: input is selected by bits R_1R_0 (pins 3-0)
$x00C_2C_1C_0$	Capacitive readout: 1 of 8 sensors selected by $C_2C_1C_0$
$x01V_2V_1V_0$	Voltage readout: 1 of 8 sensors selected by $V_2V_1V_0$

1. Building Blocks Test

VDD_d and VDDA2 are supplied with 3.3V. To tset DAC_Varef, Set Mem1(6) =1, changing Mem1(5:0). To test DAC_selftest, set Mem0(6)=1, change Mem0(5:0).
Fig. 7 and 8 show the output waveform for two DAC. Fig. 9 shows the open loop output waveform of the amplifier used in DAC.

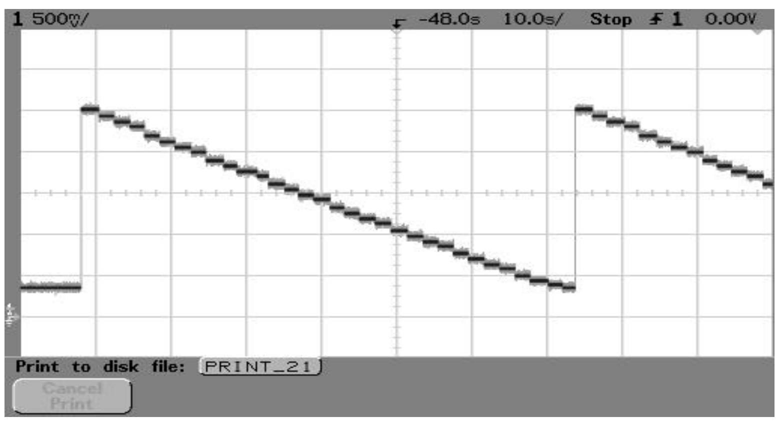

Fig. 7 Output of DAC_Varef.

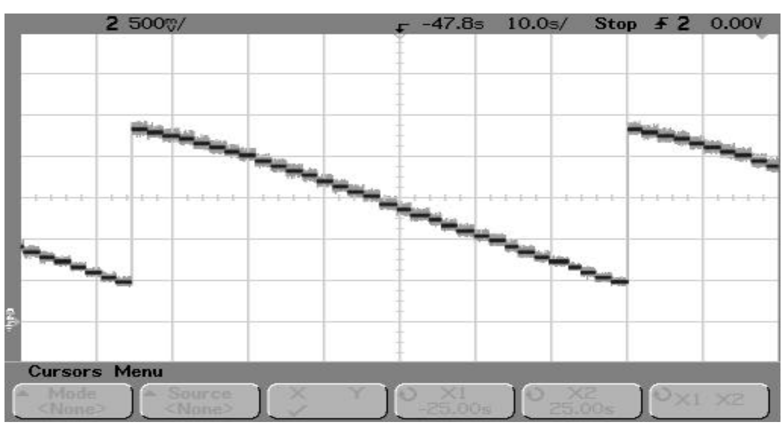

Fig. 8 Output of DAC_selftest with loading effect.

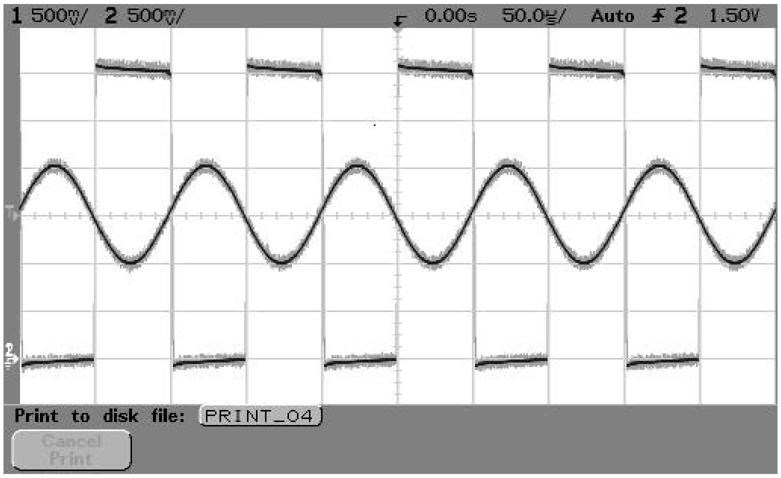

Fig. 9 Input and output of DAC amplifier (open loop).

2. Readout Test

The performance of readout has been carefully evaluated. The circuit was designated to operate with a 50 kHz clock, and both the non-overlap time of the clock phases and the clock delays were 250ns. Simulation results indicate the circuitry works from 10kHz to 100kHz. Capacitive readout measurements were performed at 50kHz while the remaining blocks were verified at 10kHz.

Voltage readout and half bridge resistive readout were evaluated by applying a 100Hz test signal to the inputs of analog signal router. Functionality of the resistive interface was confirmed. The detailed test result was submitted to ISCAS 2004. [Jichun Zhang, Andrew Mason, and Junwei Zhou, "A Configurable Mixed-Mode Multi-sensor Signal Conditional Circuit," submitted to ISCAS 2004]

SUMMARY

All the tested chips are fully functional. The fabrication support of this project from The MOSIS Service is gratefully acknowledged.