Design for MOSIS Educational Program (Research)

Design, Fabrication and Testing of a fully integrated 2.5 GHz Clock Data Recovery Circuit with Demultiplexer in 0.35 μm CMOS Process

Project submitted to MOSIS

Fabrication process: 0.35 μm

Prepared by:

Jinghua Li*, (Clock Data Recovery)

Shanfeng Cheng (Demultiplexer)

Prof. José Silva-Martínez

Texas A&M University

Analog and Mixed Signal center

Department of Electrical Engineering

College Station TX, 77843-3128

*Contact person (E-mail: jhli@ee.tamu.edu)

Aug 7th, 2003

Design Number	67125
Design Password	cdrdemux
Design Name	CDR Demux
Technology	SCN4ME_SUBM,lamda=0.2
Fabricated on Run	T34C-AK
Layout Size	1500x1500 microns
Student involved	Jinghua Li(Clock Data Recovery), Shanfeng Cheng(1 to 8 Demultiplexer)
Advisor	Dr. José Silva-Martínez

I Description of the Clock Data Recovery Circuit

The primary objective of this project is to design, layout and characterize an integrated clock data recovery circuit with de-serializer operating at a clock frequency of 2.5 GHz for OC-48 optical communications.

II Simulation and Layout Tools

The IC is designed using Cadence EDA tools. For our application, the parasitics become of extreme importance at such a high speed faster than 2.5 GHz.

III Microphotograph of the Test Chip

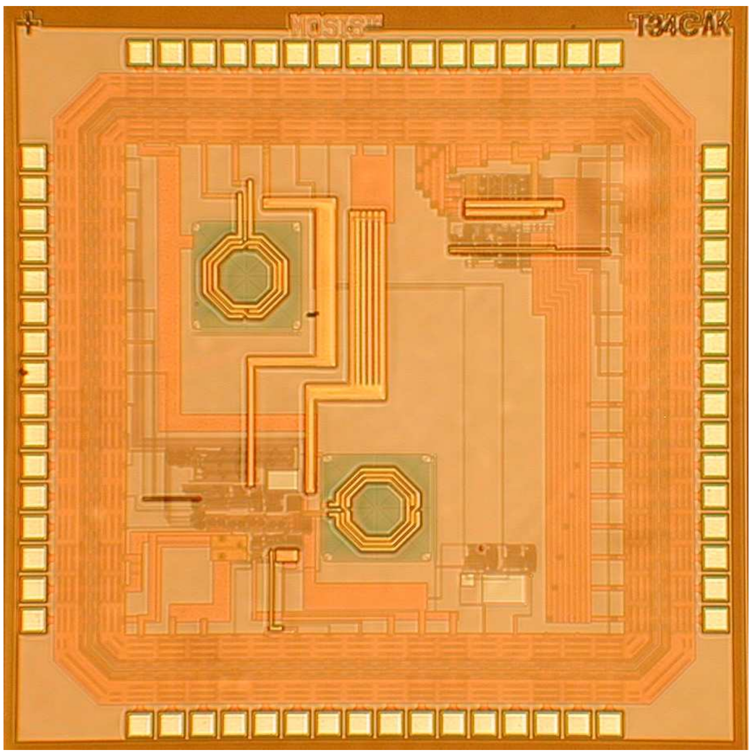


FIG 2 MICROPHOTOGRAPH OF THE TEST CHIP

IV Characterization of the Chip

In characterization of the test chip, a careful set up for measurement is needed. In high frequency the performance of the circuit become sensitive to both the resistive and capacitive loading of the measuring equipment; A printed circuit board is designed for the testing of the clock data recovery chip. The test equipment include, Rhode & Schwarz

FSEB30 20Hz~7GHz Spectrum Analyzer, Agilent Infiniium 500MHz,2Gsa/s Oscilloscope(Testing the reference clock).

As a preliminary test, two chips are characterized, both works at roughly the same frequency. Due to the over-design of the inductors(mistakenly used only half of the inductor, two inductors should have been series connected instead), half of the inductor value is used in the LC tank VCO, so the frequency is higher than expected, the VCO oscillating frequency is around 3.65GHz, matched to the design frequency times by $\sqrt{2}$.

The main limitation is that we don’t have exact modeling of the inductor. Now there is no available layout extraction software package for TSMC 0.35um CMOS technology. All this effects have resulted in the design mismatch.

The test results are attached as the following:

Fig 3 shows the frequency spectrum of the VCO output. Fig 4 shows the phase noise performance of the circuit. From the phase noise diagram, the phase noise at 1MHz away from the carrier is –105dBc.

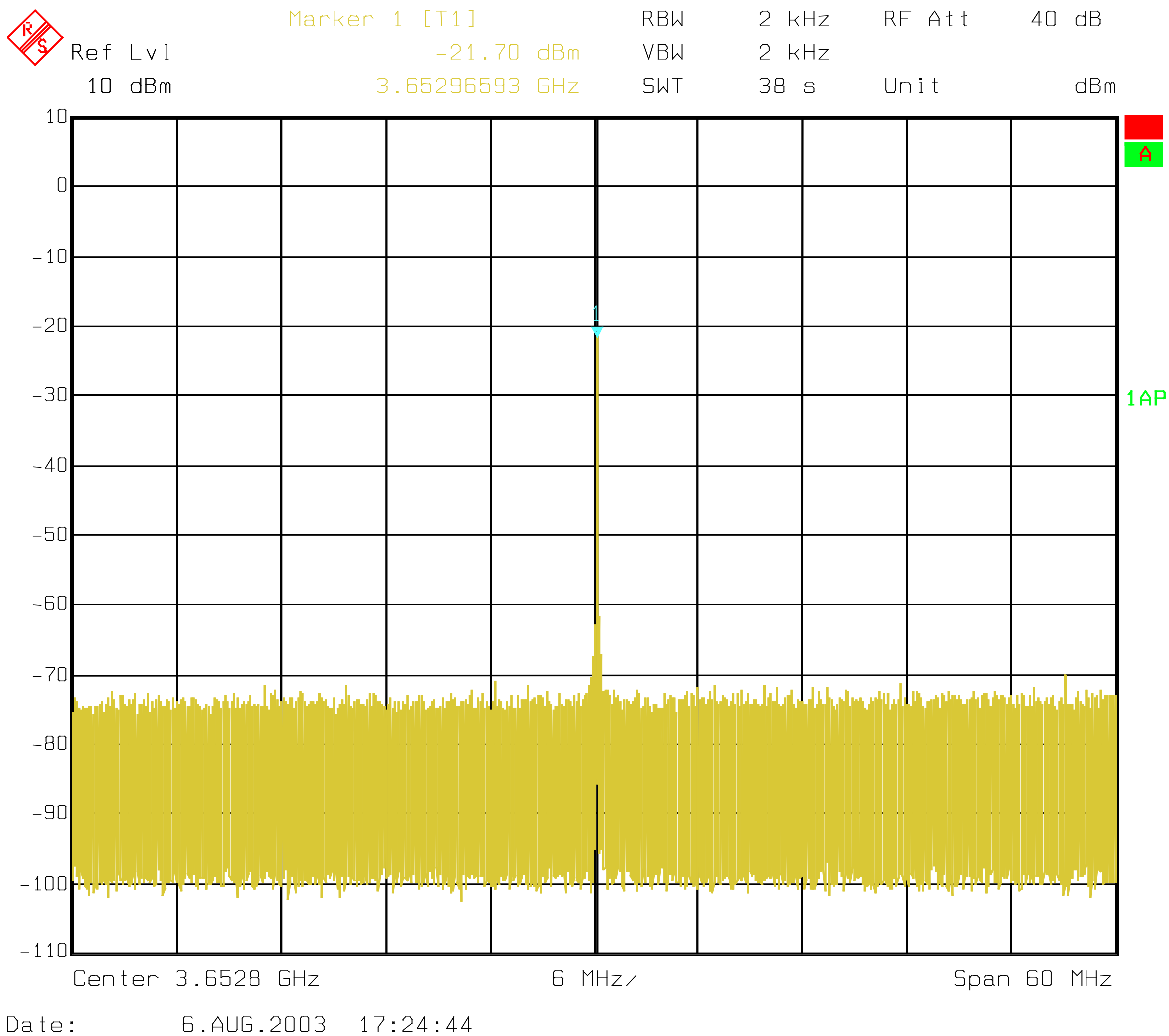


FIG 3 FREQUENCY SPECTRUM FOR THE VCO OUTPUT

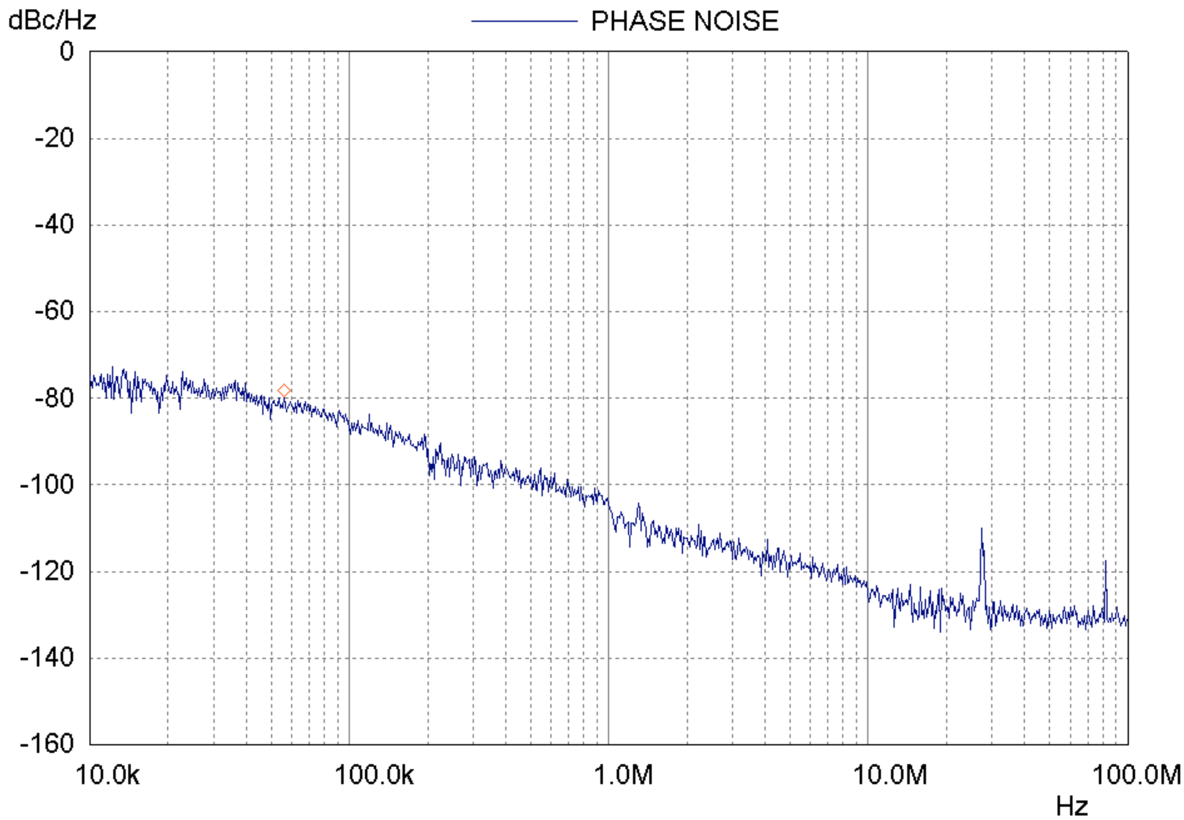
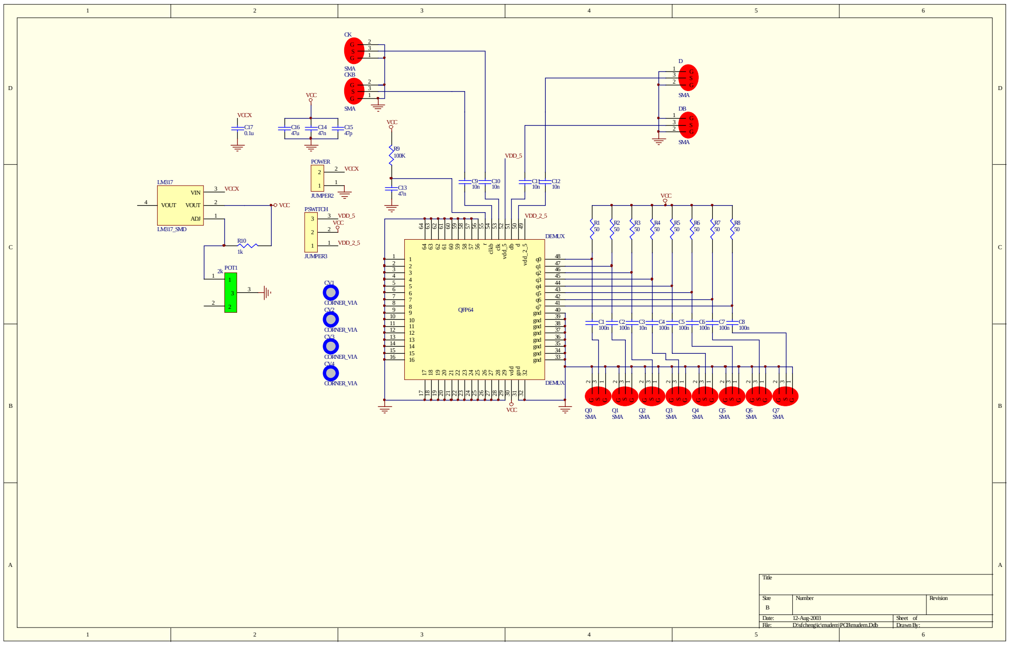


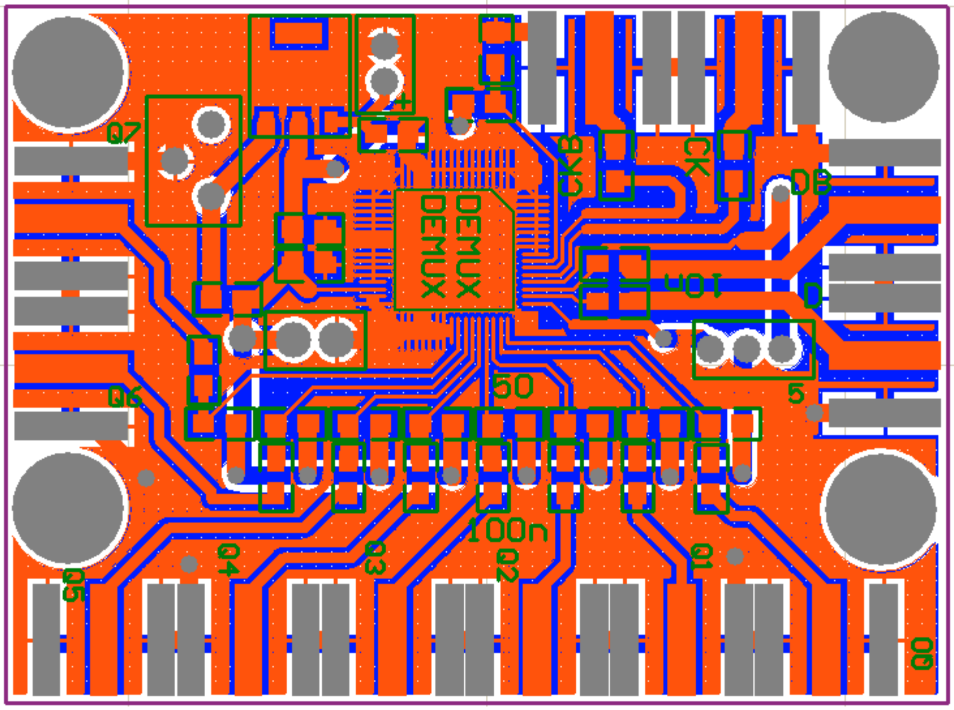
FIG 4 PHASE NOISE OF THE VCO OUTPUT

V 1 to 8 Demultiplexer Chip Testing Report by Shanfeng Cheng

1. Testing Schematic



2. Testing PCB


Q7
DEMUX
DEMUX
CKB
CK
DB
10n
D
50
5
Q6
100n
Q5
Q4
Q3
Q2
Q1
Q0

3. Test results

We use full differential input for both clock and data. For both input clock and data, the differential 50ohm input matching resistors are built on-chip. So there are no resistors on the input side. Only DC-block capacitors (10n). For the output side, there are 8 output streams since it's a 1 to 8 demultiplexer. The output signals are all single-ended with a peak-peak swing of 400mV. Each output pin is connected to a 50ohm pull-up resistor, then connected to a DC-block capacitor and then connected to 50ohm termination (oscilloscope probe) by way of SMA connector.

Due to the limitation of the operation speed of the signal generator in our group (Analog & Mixed Signal Center of Texas A&M University), the highest input data rate is 660Mbps and the corresponding clock frequency is 330MHz for proper demultiplexing.We were able to verify the function of this chip but not able to measure the highest performance of this chip (this chip can accommodate an input data rate of 5Gbps). The full chip characterization will be done soon at the XILINX facilities in Austin.

The function of the chip is verified to be correct by the following method. We input a fixed 32-bit length input data pattern (i.e., the pattern repeats every 32 bits). We've observed that all the outputs are repeating every 4 bits exactly as expected. What's more, when we reassemble the 8 outputs, the assembled pattern is the same as the input pattern in a cyclic manner (i.e., 1234567 is considered the same as 2345671 in a cyclic manner)

Minimum Input Data Swing (Vpp)	0.38V
Minimum Input Clock Swing (Vpp)	0.41V
Verified Working Frequency Range	10MHz – 660MHz

We are going to redesign a better board and test with better equipment in XILINX to further characterize the highest performance of the demultiplexer. We will submit another more detailed report when we get new results.