

Design, Fabrication and Testing of a fully integrated 2.5 GHz Clock Data Recovery Circuit in 0.35 μm CMOS Process

Project submitted to MOSIS

Fabrication process: TSMC 0.35 μm

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The Synchronous Optical Network(SONET) protocol has become the standard in optical communications used in WANs. SONET specifies a set of transmission speeds, all of which are multiples of “OC-1” rate, which is 51.84 Mb/s. Currently OC-48, running at approximately 2.5 Gb/s, are being deployed throughout North America. A typical OC-48 transceiver is shown in Fig 1.

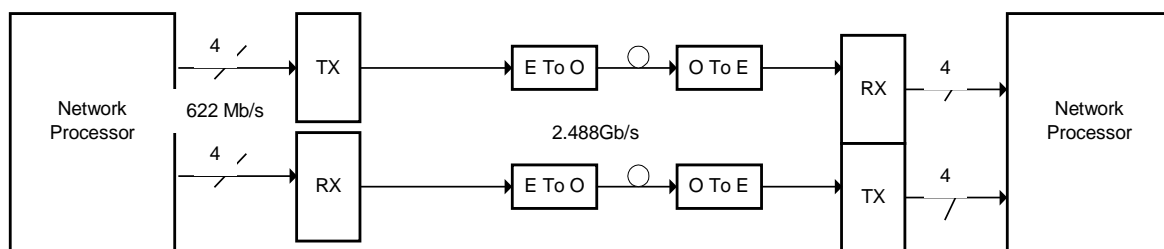


Fig 1 OC-48 Transceiver Architecture

A network processor will convert input data into the form of four parallel signals, each operating at 622Mb/s. These signals are sent to the parallel inputs of the transmitter where they are synchronized to a precise reference clock and then serialized so that the output of the transmitter is a single channel operating at 2.488Gb/s. The high speed serial transmitter output is used to modulate a laser driver, which generates the optical signal that is sent through a fiber. At the receiving side of the fiber, the light is applied to a photodiode connected to a transimpedance amplifier(TIA) which then converts the signal back into

electronic form. The electronic signal is applied to a post-amplifier and then a limiting amplifier before it is applied to the receiver input. In the receiver a clock synchronized to the incoming data is generated using a clock data recovery (CDR) circuit. The recovered clock and re-timed data provided by the CDR are then applied to a demultiplexer with four parallel output signals, each at 622Mb/s. These signals are applied to the network processor which performs the necessary overhead and framing operations.

The primary objective of this project is to design, layout and characterize an integrated clock data recovery circuit with de-serializer operating at a clock frequency of 2.5 GHz for OC-48 optical communications. The main focus in this project is to use two loops for fast acquisition and large pull-in range of the phase locked loops. To overcome the ripple of the control line of the charge pump, a continuous-time phase detector and Gm Cell will be used in the second loop to suppress the glitches on the VCO control node due to the charge pump. This method is robust for data recovery systems and will be widely used in future applications. Traditional CDR schemes use bipolar technology or GaAs BiCMOS technology, which are very expensive for commercial applications. In our proposed scheme, we use CMOS technology to construct the prototype chip, a digital lock detector and digital/analog phase detector will be used to monitor and sense the variation of the frequency and phase difference. This results in improved performance and ease the design challenge.

The clock data recovery chip will be designed with the trade-off between the jitter generation(output jitter should be less than 4ps rms) and jitter transfer specification, and pull-in range will be also optimized. Extensive Matlab and Simulink simulations have been done to test and evaluate the performance of the topology, stability, loop bandwidth and phase noise have been optimized as well. The components that are going to be integrated in the design include phase frequency detector, charge pump, VCO, Phase detector, analog Multiplexer and high speed de-serializer The output bitstream will be analyzed HP analyzer and a testfixture off the chip.

The design tools we have in our group include Cadence IC446, LDV31 tools along with the NCSU CDK design kit.

The design is being simulated using SpectreS simulator with the Analog Artist Environment of Cadence. This will be done using the SPICE model parameters provided by MOSIS for the TSMC 0.35 μ technology. Monte Carlo simulation using Analog Artist is also required to be sure that the design is robust enough to meet the specifications under normal manufacturing process variations. This will provide us with an estimated distribution of the values of the most important specifications as a function of the statistically varying device model parameters.

A layout of the final design will be created using Virtuoso Environment of Cadence. Good layout techniques such as common-centroid arrangements and dummy transistors should be used for better matching. This is mainly done to average the process parameter gradient over the area of the devices to be matched. The LVS (Layout vs. Schematic)

checker tool of Cadence will be used to ensure that both the extracted layout and the schematic are matched. For our application, the parasitics become of extreme importance at such a high speed at 2.5 GHz. So it become a must in this stage to perform post layout simulations of the design using the extracted layout including the parasitics rather than the circuit schematic used in the first stage of the design. This will give us a prediction of the effect of the parasitic capacitors on the performance of the design.

It is also important to point out that we are also intending to include in our layout, besides the main design, an LC-tank VCO to test the substrate effect on the quality factor (Q factor) of the inductor. This will allow us to analyze the effect of Q value of the inductor.

The final stage will be the experimental characterization of the fabricated chip. A careful set up for measurements is needed. In high frequency the performance of the circuit become sensitive to both the resistive and capacitive loading of the measuring equipment; on-chip buffers carefully designed will be used. A printed circuit board will be designed for the testing of the clock data recovery chip. The chip will be tested under 2.5GHz clock speed using HP test package.

The estimated area of the chip is $3.5 \times 3.5 \text{mm}^2$, and we plan to use a 64-pin PTQFP64A package for the chip.

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