

Development of Multi-Technology FPGA Incorporating Photonic Information Processing Block Subsystem

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Introduction

The second phase of the MT-FPGA project was an attempt to demonstrate the functionality of a small array of Multi-Technology Logic Clusters (MTLC) and the supporting programmable interconnect. The 7mm² of floor space allowed for a 3 by 3 array of MTLC to be integrated into the design. Also, included in the design were a number of independent test structures to isolate certain features from the rest of the project. The MT-FPGA project was carried out as a modular design featuring several major sub-blocks that were each responsible for a specific aspect of the system's overall operation. Figure 1 shows all of the major design components and gives some idea of the high level connections between these components and Figure 2 shows the layout as it appeared just prior to tape out. The array of MTLC blocks have the ability to arbitrarily communicate with each other and the outside world through the Routing Channels, Switch Blocks (SB) and I/O Blocks that move all the data around within the MT-FPGA. At the center of each MTLC, there is a reserved space that is designated for use by a Multi-Technology Block (MTB). This MTB can take on any form so long as it is compatible with the process technology and can operate by using the 2 digital and 2 mixed-signal routing channels available for 2 way communication between the MTCL and the MTB. This design featured two different photonic information processing MTB blocks one of which is an optical power meter and the other is a photoreceiver system with a digitally programmable optical threshold.

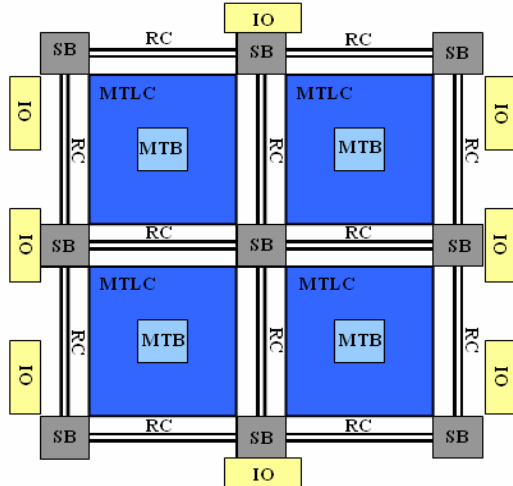


Figure 1: High Level Architecture of MT-FPGA

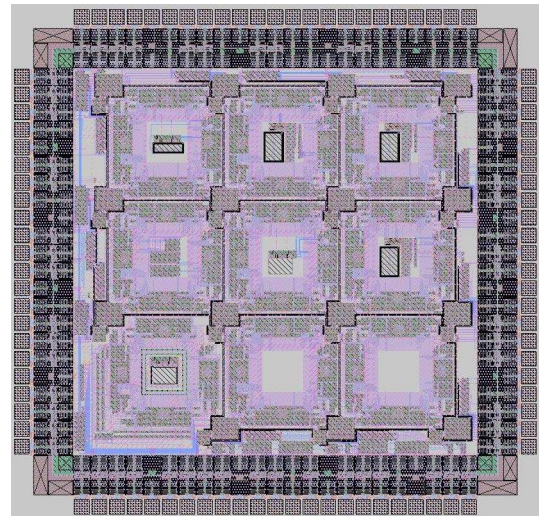


Figure 2: Final design layout

Test Results

The testing of this design has been greatly limited because of a design error which was discovered in the layout. The critical design failure in the area of FPGA programmability severely impacted functionality and testability. The error was in the design layout and affected all the devices. Specifically, the shift register meant for shifting in the FPGA configuration data had a routing error that prevented it from working properly. The error occurred at the sixth element in the chain of 98 elements. As a result less than 10 percent of the memory elements on the FPGA were controllable. Pre-fabrication simulations of the

particular area of the design were overly simplistic and did not catch the error. A few simple test cases that operated entirely within the functioning area were still possible. Fortunately, the error did not influence the independent test structures so some results were still able to be gathered.

Routing Channels and I/O

Widespread testing of the FPGA was not possible because of the limited programmability, however, simple test cases for the routing channels and I/O blocks on the extreme left hand side of the layout were still possible since the leftmost switch blocks, routing channels and I/O blocks were all in the area of the chip functioning properly. As a result, the delay and performance could be measured for an analog pathway traveling into the chip through one I/O block through a switch block to a routing channel and then back out of the chip through another switch block and I/O block. Figure 3 shows the pathway.

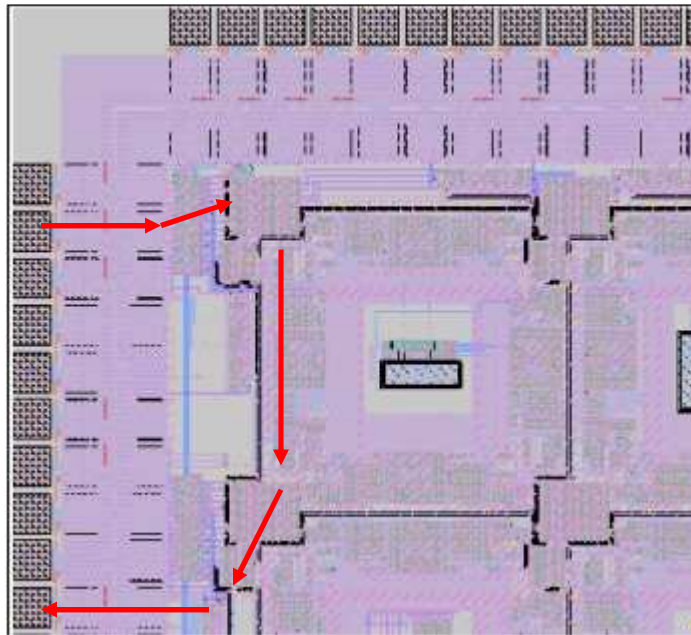


Figure 3: A testable pathway.

Analysis of the pathway shows analog signal transmission through the channel up to 700 KHz with a delay of approximately 80 ns. Figure 4 shows the results of an AC sweep through the channel.

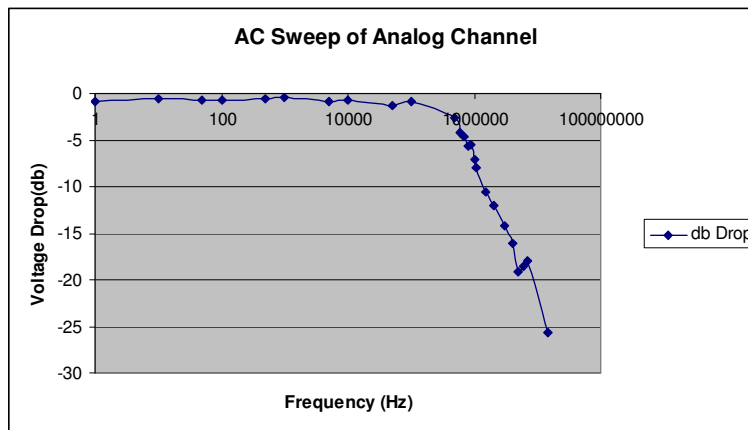


Figure 4: Analog routing channel performance.

Independent Sub-Block Testing

Two major independent sub-blocks were also included in the design. The first was a fully isolated set of MTB optical power meters, and the second was a complete MTLC. Each of these test features has been successfully characterized. Figure 5 shows a block diagram of the isolated MTB subsystem.

There are two MTB that are testable. One is configured for full optical mode and the other is configured in electrical mode. A number of devices were characterized on each setting. In optical mode, the input optical power from a 852 nm laser source was swept and the resulting VGA output and 4-bit digital power output were recorded. Electrical testing was done in the same way. Table 1 contains a record of the power consumption and biasing conditions for seven chips. Figure 6 shows the output of the VGA at a variety of photoreceiver gain settings, and Figure 7 shows the complete set of output data for a single sweep of the optical power.

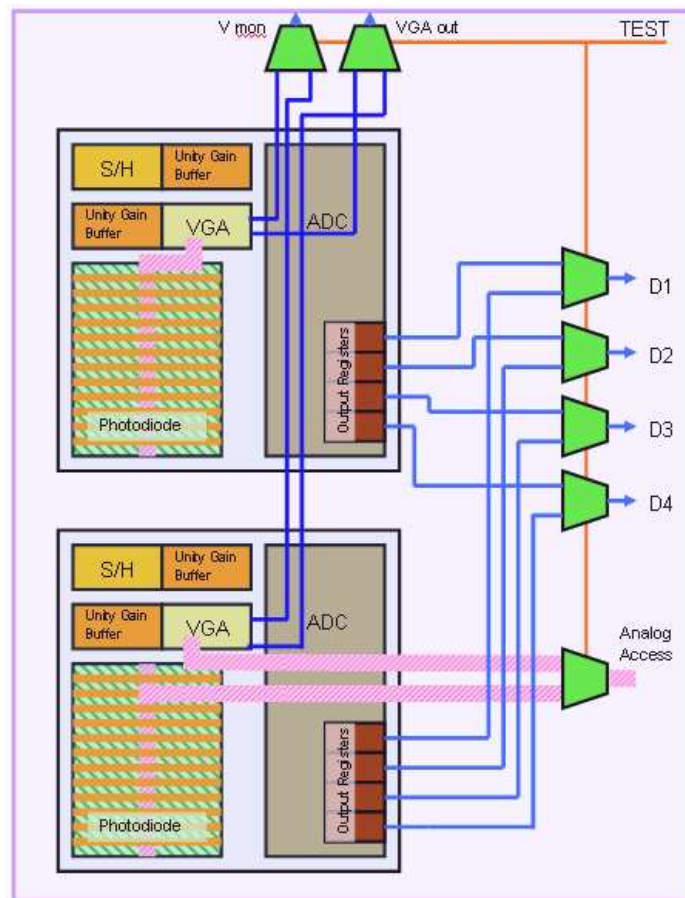


Figure 5: MTB test structure.

Table 1: Chip power consumption and biasing

	Vbias(V)	Vgain(V)	I power Supply(A)	Power(mW)
Chip 1	1.188	3.01	0.08	264
Chip 2	1.185	3.08	0.08	264
Chip 3	1.197	3.11	0.07	231
Chip 4	1.199	3.04	0.08	264
Chip 5	1.185	3.02	0.07	231
Chip 6	1.19	3.05	0.07	231
Chip 7	1.212	3.08	0.07	231

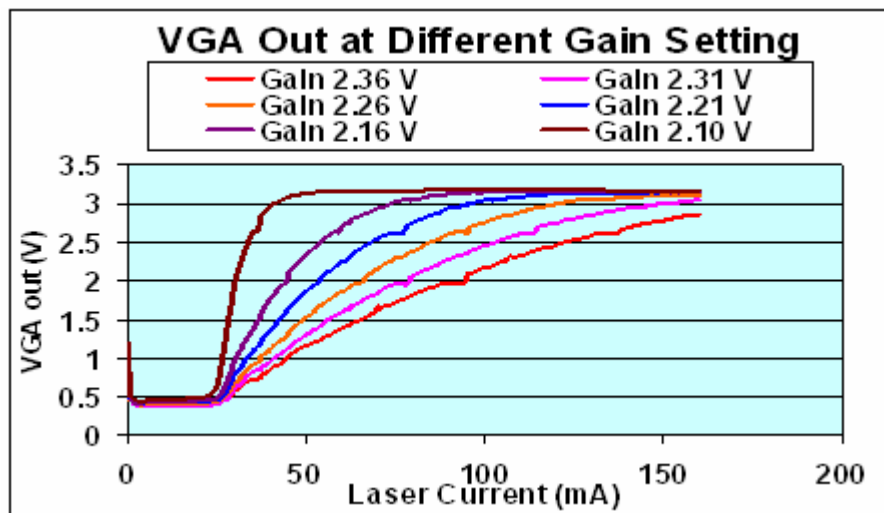


Figure 6: VGA outputs.

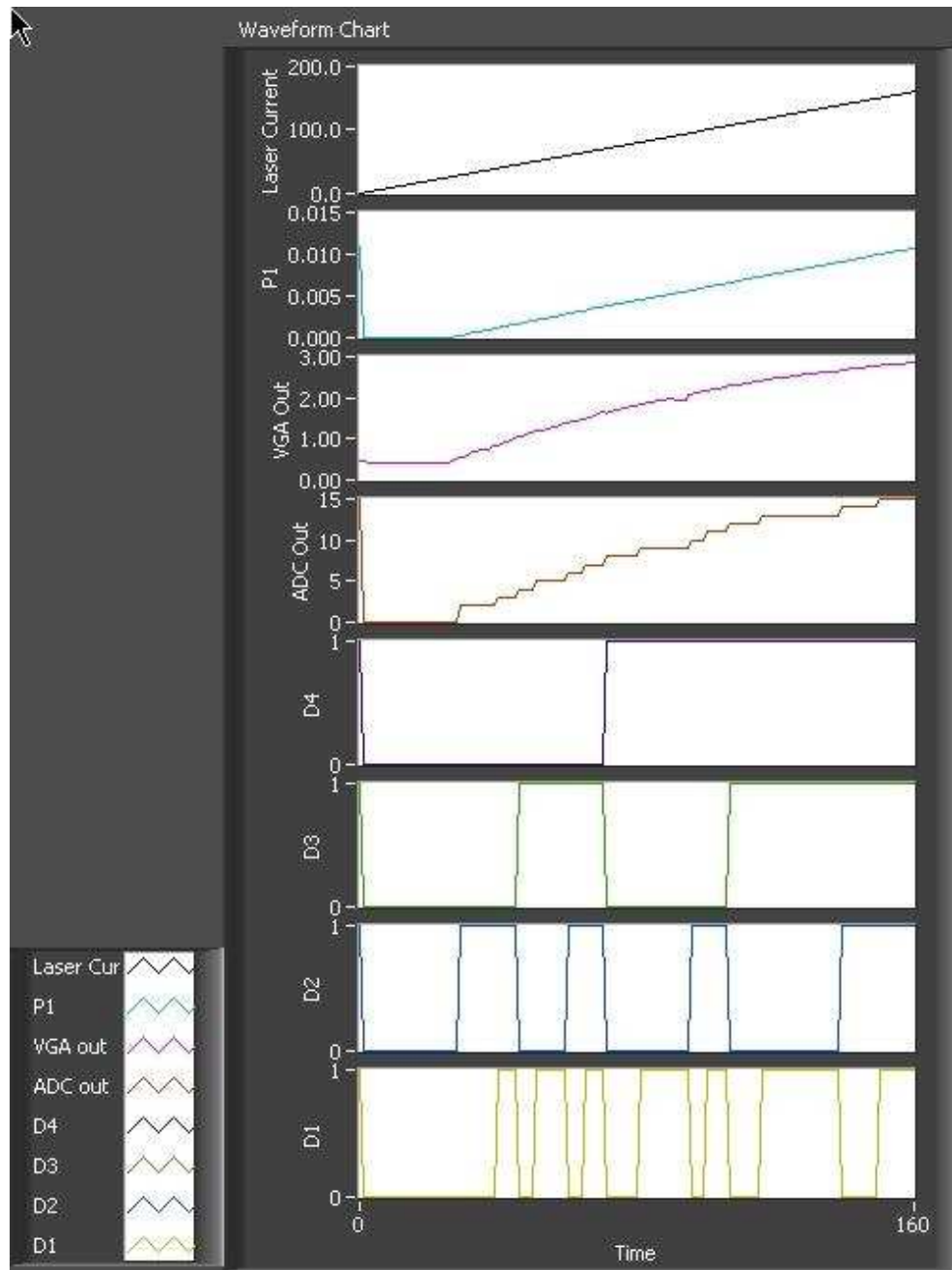


Figure 7: A single sweep of the optical power meter.

Aside from the MTB test structure, there was also a complete independent MTLC featuring its own independent configuration chain. As a result, this MTLC was still testable allowing for it to be full tested and characterized. A summarization of these results is visible in Table 2 and Table 3. Table 2 gives results pertaining to the MTLC itself, and Table 3 shows the delays associated with a connection block used for joining an MTLC to a routing channel.

Table 2: Specifications of an MTLC

Figure of merits Of an MTLC	AMI 1.5 μ m Technology		TSMC 0.35 μ m Technology	
	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
Inverter (Propagation delay)	26ns	25ns	9.6 ns	6 ns
Average propagation delay	$(26+25)/2ns = 25.5ns$		$(9.6 + 6)/2ns = 7.8ns$	
Ring Oscillator(3-invert Frequency	$f_{oscillation}$ =		$f_{oscillation}$ =	
2-firm links and 1-soft link	12.12 MHz		64.9 MHz	
1-firm link and 2-soft links	10.75 MHz		60.9 MHz	
Time Penalty for replac one firm link with soft link	$t_{pen} = (73ns - 62ns) = 11 ns$		$t_{pen} = (16.4 - 15.4) ns = 1 ns$	
Power consumption Per MTLC without a Multi-tech block	< 25mW			
Testability of Several Scan chains	All worked as expected		All worked as expected	
Other test cases	1) Demonstration of a clocked synchronous finite state machine(CS-FSM) 2) Combinational logic		1) Demonstration of a clocked synchronous finite state machine (CS-FSM) 2) Combinational logic	
Example circuits implemented	1) 1-bit slice pipelined full adder → capable of adding two continuous serial bit streams 2) Different Combinational functions involving NAND/NOR/ complement		1-bit slice pipelined full adder → capable of adding two continuous serial bit streams 2) Different Combinational functions involving NAND/NOR/complement	

Table 3: Specifications of a connection block.

Figure of merits Of a connection bloc	TSMC 0.35 μ m Technology			
	Digital part		Analog part	
Inverter (Propagation delay)	t_{pLH}	t_{pHL}	t_{pLH}	t_{pHL}
	11 ns	7.8 ns	14.6	8.4 ns
Average propagatio delay	$(11 + 7.8)/2 ns$ =9.4 ns		$(14.6 + 8.4)/2 ns$ =11.5 ns	
Time Penalty	Δt_{pLH} =1.4ns	Δt_{pHL} =1.8ns	Δt_{pLH} =5ns	Δt_{pHL} =2.4ns
Average Time Penal	$\Delta t_p = 1.6ns$		$\Delta t_p = 3.7ns$	

