Development of Multi-Technology FPGA Incorporating Photonic Information Processing Block Subsystem

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1. INTRODUCTION

Since their introduction in 1985-86[1], Field Programmable Gate Arrays (FPGA) have been developed into a major device technology that is suitable for applications requiring programmable/reconfigurable digital logic. Many different architecture and programming technologies have evolved to provide better designs that make FPGA technologies economically viable and an attractive alternative to Application Specific Integrated Circuit (ASIC's) [2]. One limitation of current FPGA's is that the user is limited to strictly electronic designs. Thus, they are not suitable for applications that are not purely electronic, such as optical communications, photonic information processing systems [3] and other multi-technology applications. The integration of these technologies requires a new kind of FPGA that merges conventional FPGA technology with mixed signal and other multi-technology devices. This new class of field programmable device will extend the flexibility, rapid prototyping and reusability benefits associated with conventional electronic into the multi-technology domain enabling the development of a whole new class of integrated and embedded systems.

To demonstrate the feasibility of Multi-technology FPGA, a new FPGA architecture is proposed here. This MT-FPGA can exploit the capabilities of both traditional FPGA's and the ability to work outside the electronic domains with multi-technology device capabilities. The FPGA architecture presented here allows for the incorporation of a variety of multi-technology blocks like optical blocks, Analog-Mixed-Signal blocks, RF blocks, SRAM blocks, MEMS blocks, chemical/biological sensor blocks, etc.. Since the implementation resembles a conventional FPGA; the idea is robust and scalable. Further, existing high-level CAD tools can be readily modified to provide a CAD environment that is comparable to existing technology. In this design, a smart photoreceiver for photonic information processing is used as a vehicle to demonstrate the functionality of the proposed MT-FPGA.

2. PROJECT DESCRIPTION

We present here the design and implementation of a new multi-technology FPGA architecture. In this novel architecture, we use a modular approach where each multi-technology block will be surrounded by electronic programmable logic blocks (PLB's) with an internal bus for communication internally within the cluster and externally with the routing channels.

Figure 1 illustrates the high level architectural definition of the proposed MT-FPGA. The array of blocks resembles the symmetrical array used in the layout of electronic FPGA's where each logic block is replaced by a cluster of blocks consisting of a multi-technology block (MTB) and four Programmable logic blocks (PLB's). This cluster is called a multi-technology logic cluster (MTLC). The regular array of MTLC is interspersed with horizontal and vertical routing channels. Routing segments are connected in programmable fashion through the Switch blocks (SB). The inputs and outputs of different MTLC's can be connected to the routing channels in configurable ways using the connection blocks (CB). The floor plan of a MTLC (Figure 2) shows that each MTLC is made up of four PLB's surrounding a single Multi-technology block. The MTB may contain one to several multi-technology devices (ex. Photonics, MEMS,

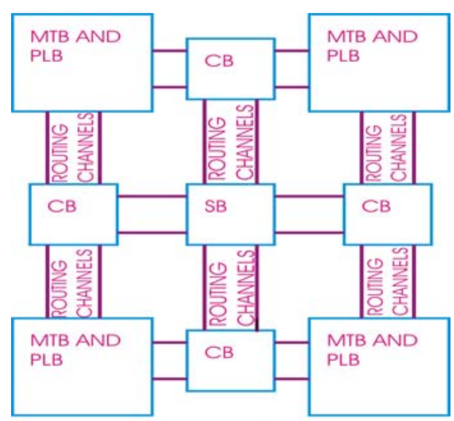

Figure 1 Generic block diagram of the proposed multi-technology FPGA.

etc.). As indicated in Figure 2 the four PLB's communicate with the multi-technology block (and each other) using a 16-bit internal bus. MTB's are hybrid technology blocks that may be required to exchange raw and/or processed data with PLB's using a set of programmable connections. The 16-bit internal bus is subdivided as follows:

• 4-bits are used for output signal distribution from PLB's.
• 4-bits are designated for two-way communications with MTB.
• 4-bits are dedicated for signals coming from other MTLC via the routing channels and controlled by programmable switch blocks.
• 4-bits are used for clock distribution, reset signal & configuration enable.

Like conventional FPGA's, the trade-off between area and density is an important issue in this design. Chow et.al.[5,6] have addressed this problem in conventional FPGA's and shown that in conventional FPGA's , the use of hard-wired logic blocks (HLB) using an L3-4.2 tree topology significantly improves speed and area utilization of a conventional FPGA architecture.

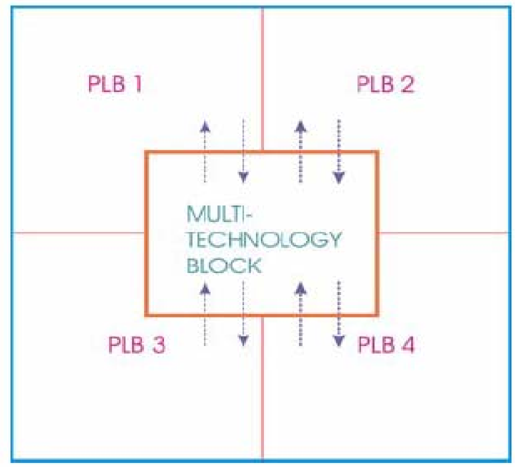

Figure 2 Floor plan of a typical MTLC showing 1 MTB surrounded by a four PLB cluster.

3. PROJECT COMPONENTS

Aside from the MTLC, there are three additional subsystems of the MT-FPGA that warrant further description. Each component presented challenges in extending the traditional FPGA design to accommodate the presence of mixed technologies.

3.1 SMART-PHOTORECEIVER DESIGN FOR THE MTB

For this design the MTB block space will be occupied by a Smart-Photoreceiver. Each MTLC is paired with a single MTB block. The Smart-Photoreceiver system detects an incident light source and quantifies its optical intensity. The process begins with a photodetector that collects optically generated carriers and generates a photocurrent. This current is then sent to a variable gain transimpedence amplifier where the signal is amplified so that it can be input to a 4-bit Flash ADC. The ADC completes the signal transformation and outputs the digitized optical power to the internal bus of the MTLC.

For this system to work properly, the Photoreceiver requires two analog voltage inputs to be adjusted in a way to achieve the desired system performance. The first signal, V-gain-control, increases or decreases the Photoreceiver gain. This allows flexibility for the user to choose between greater resolution or greater range of valid inputs. Once the gain is set, the V-bias signal can be adjusted to calibrate the digital ADC values. In other words, the window of signals within the range of the ADC can be shifted to higher or lower optical power ranges. Figure 3 illustrates the design of the photreceiver system.

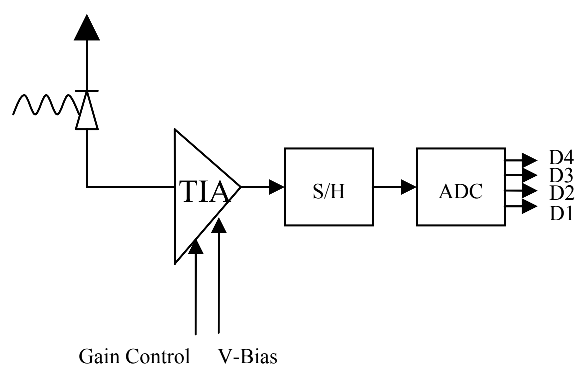

Figure 3: Block Diagram of MTB Smart Photoreceiver System.

3.2 SWITCH BLOCK DESIGN

One of the major components of the MT-FPGA is a Switch Block capable of controlling the signal routing of both the analog and digital signals as they are distributed around the chip. In doing so, every effort must be made to reduce the signal degradation of the signals, and in particular to protect the sensitive analog pathways. This block will attempt to utilize appropriate strategies for isolating these analog signals such as physical partitioning between analog and digital signal, placement of guard rings, and the use of metal shielding.

One major problem with using SRAM based analog interconnect strategies is the high resistances associated with such segmented routing structures. This design will also seek to find strategies to mitigate the effects of this problem.

4. AREA ESTIMATION

The project is intended to implement a 2x2 array of MTLC blocks. Each MTLC block will require 3300 by 3300 λ. The Switch Block in the routing channels between each MTLC block requires an additional 900 by 900 λ. Combined the MTLC and Switch Blocks make for a core area of 7500 by 7500 λ. Surrounding this core is the pad frame and a ring of I/O routing blocks. Accounting for these structures the total design should require about 11,100 by 11,100 λ or 2,220 by 2,220 microns.

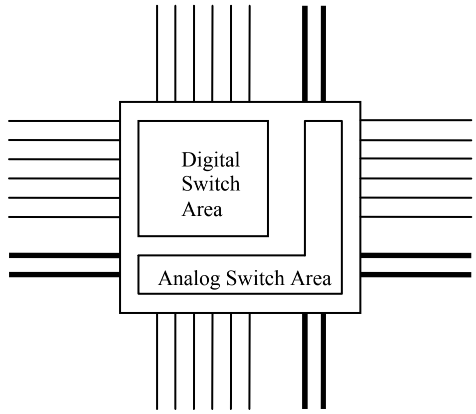

Figure 4: Illustration of Switch Block Structure.

5. REQUESTED RESOURCES

To successfully demonstrate the viability of our design, we request a chip area of 2.64 mm x 2.64 mm = 7mm^2 on a future MOSIS run of the TSMC35_P2 process. All other resources necessary for the design and test of the proposed chip are available in the Photonic Systems Development Lab and The University of Cincinnati

6. PROJECT TIMELINE

Design Specification	**9/15/02**
PLB Design and Layout	**2/24/03**
MTB System Design and Layout	**2/24/03**
Switch Block Design and Layout	**2/24/03**
I/O Block Design and Layout	**2/24/03**
System Integration and Routing	**2/27/03**
Simulated Testing and Evaluation	**3/3/03**
Submission to MOSIS	**3/10/03**
Test Setup and Preparation	**5/17/03**
Chip Return from MOSIS	**5/21/03**
Chip Testing	**6/12/03**
Feedback Report to MOSIS	**6/26/03**

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