

Design Report for MOSIS Educational Program (Research)

**A Deterministic Dynamic Element Matching Approach
for Testing High Resolution ADCs Using Low Accuracy DACs**
(Design Number: 68091)

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Performance Summary

Design number: 68091

Design name: DDEMDAC_ISU

Technology: SCN3ME_SUBM, $\lambda = 0.3$

Fabrication ID: T37DBP (AMI_C5F)

This is an test report of a design that was fabricated via the MOSIS Educational Program in July 2003 (Design number 68091). The design was functional and validated the proposed Deterministic Dynamic Element Matching (DDEM) method. With the 8-bit DDEM DAC, we can test 11-bit ADCs with test error bounded by half LSB. However, the performance was not as good as expected. It has been characterized that the major performance degradation results from the power supply voltage variation over the whole chip due to un-well-managed power supply routing. Besides, the previous design is only an 8-bit DAC, and the performance is limited by its resolution. A new design of 12-bit DDEM DAC with improved power supply routing has been finished and will be submitted for re-fabrication.

A Deterministic Dynamic Element Matching Approach for Testing High Resolution ADCs Using Low Accuracy DACs[†]

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Abstract

This paper presents a Deterministic Dynamic Element Matching (DDEM) approach which is applied to low precision DACs to generate stimulus signals for ADC testing. Both simulation results and experiment results from a fabricated DDEM DAC are presented to verify the performance. The effective performance of an 8-bit DDEM DAC (linearity less than 8 bits without DDEM) is comparable to what is achievable with a 12~13-bit linear DAC. This technique offers potential for use in both production test and BIST environments.

1. Introduction

The most common and widely used mixed-signal circuits are digital to analog converters (DACs) and analog to digital converters (ADCs) [1]. Data converters are widely used because they serve as the interface between digital logic and the analog or physical world. Due to increasing resolution and conversion rates, the challenge and cost of testing analog to digital converters (ADCs) is growing. Testing techniques that facilitate a reduction in the cost of test or that support Built-in-Self-Test (BIST) will have a significant impact in the final product costs [2].

BIST structures for analog and mixed-signal circuits offer the potential to reduce cost while also providing a capability to test deeply embedded systems on a chip (SOCs). BIST schemes can also be used for self-calibration [3] and hence improve circuit performance. Most existing approaches have been aimed at duplicating a standard tester on chip [4-11], which leads to producing a highly accurate and linear stimulus on the chip. However, the prior arts have not demonstrated linearity adequate for testing high resolution ADCs on a BIST application.

A different approach had been introduced recently [3] [12-14], where the linearity requirements on the signal generator are relaxed by using multiple inputs and signal processing techniques to accurately characterize the DUT. In this paper an alternate approach is proposed by using DDEM on low linearity DACs to generate a statistical linear source that can be used to test highly-linear ADCs. No signal processing is needed and we can use the already available code-density techniques to obtain the measurement.

DACs are commonly used to generate the input signals needed to test ADCs and the performance of most useful DAC architectures is dependant on the matching properties of critical elements. Due to process variation, element matching errors are inevitable. Although special layout techniques, special processes, and/or laser trimming can be used to reduce matching errors, these methods lead to significant cost increases and are difficult to use on BIST. The existing DEM technique [15] [16] property accepts matching errors as inevitable and dynamically rearranges the interconnections of the mismatched elements so that on the average all element values are nearly equal. The DEM method was first introduced by Van De Plassche in 1976 [15], and then was used by H. T. Jensen and I. Galton [17] [18] to improve the effective specifications of linearity performance of DACs. It has been demonstrated that DEM can be used to appreciably improve the SFDR performance of moderately low-linearity DACs [17] by spreading the errors in the DAC over a wide spatial frequency spectrum. This behavior is a direct consequence of the randomizing effect provided by DEM.

Other researchers [19-24] have used DEM in Delta-Sigma Converters and the high oversampling ratio inherent in these structures can either partially or totally remove the limitations associated with the time-local errors. B. H. Leung and S. Sutarja presented three different approaches to DEM in [19]: Conventional Random Averaging, Clocked Averaging and

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Individual Level Averaging. The DEM was applied on a 3-bit DAC in a Delta-Sigma ADC. R. T. Baird and T. S. Fiez introduced and analyzed in [20] the Data Weighted Algorithm (DWA). Different modifications to the DWA are made on [21-23] to improve its performance. Adams and his colleagues present a Data-Directed Scrambler for multi-bit noise shaping D/A converters in [24]. Most of these DEM algorithms are input data dependent and are variants of the Data Dependant First use-Next use (DDFN) algorithm. None of these algorithms have been used for testing purpose and many problems are involved in these algorithms, such as the spectral spurious components generated by DEM, the large sampling window required and the time-local non-stationarity. Here we will introduce a new DDEM algorithm which is applied to ADC test, where such problems do not affect the test performance.

Our application of DDEM allows the signal generator to be realized with a low-linearity DAC, eliminating the need of large silicon area and reducing the design requirements of the test signal generator. A preliminary theoretical study investigated the use of random DEM with a highly-nonlinear DAC to test low-resolution ADCs [25]. The idea behind DEM testing is to generate the ADC stimulus with more than one DAC output sample for a given DAC input digital word; each sample is generated using different elements following the DEM philosophy. Since DEM is used in the input signal generator we do not have to worry about DEM in the signal path. DDEM was introduced, compared to the random DEM testing and theoretically analyzed in [26-28]. It was shown that the DDEM significantly outperformed RDEM for a given number of samples per DAC code.

This paper is organized as follows. Basic notation on INL characterization is given in Section 2. Details are presented in Section 3 about the DDEM DAC structure, DDEM algorithm description and theoretical performance evaluation. In Section 4 simulation results of testing 11-bit and 12-bit resolution ADCs using an 8 bit DDEM DAC are presented. An 8-bit DDEM DAC design and the experimental results are presented in Section 5.

2. INL Characterization

There are several alternative but similar definitions of the INL of an ADC. Some authors [29] define an INL function as a continuous function of the ADC input voltage, $INL(V_{in})$. Also some authors define an INL function from a discrete sequence denoted as INL_k determined by the transition points of the ADC while others define an INL function from a discrete sequence of output code densities obtained by exciting the ADC with a known test signal such as a ramp or sinusoid. In all cases, the INL is defined to be the maximum magnitude of either the continuous or discrete INL functions and there is usually not much difference in the INL obtained from any of the three definitions. In this paper, we follow what is the most common INL definition used by test engineers in industry. Specifically, the transition point, T_k , will be first estimated from code density outputs of the DUT generated from a characterized input signal. The INL_k of an ADC is defined relative to a fit line to the actual transfer characteristics. The fit line is usually the end point fit line. If we define n to be the resolution of the ADC and let $N=2^n$, an ideal n -bit ADC will have $N-1$ uniformly spaced transition points. If there are no missing codes in the ADC output, the non-ideal ADC will have transition points at T_1, T_2, \dots, T_{N-1} . The $N-1$ uniformly spaced points on the end-point fit line are denoted by $\underline{T}_1, \underline{T}_2, \dots, \underline{T}_{N-1}$ and are related to the actual first and last transition points by the expression:

$$\underline{T}_k = T_1 + \frac{T_{N-1} - T_1}{N-2}(k-1), \quad k = 1, 2, \dots, N-1 \quad (1)$$

The pair-wise difference between the actual transition points and the fit-line transition points is defined as INL_k and is expressed in LSBs as

$$INL_k = \frac{T_k - \underline{T}_k}{1 \text{ LSB}} = \frac{T_k - T_1}{T_{N-1} - T_1} (N-2) - (k-1), \quad k = 1, 2, \dots, N-1 \quad (2)$$

Since the fit line is the end-point fit line, $INL_1 = INL_{N-1} = 0$.

A linear ramp is widely used in industry as the input signal to the ADC under test and the numbers of occurrences of each ADC output are tallied into corresponding code bins. Notationally, H_k is the number of occurrences of code k . Since V_{in} is proportional to time and the sampling intervals are constant, the total number of accumulated samples for a linear ramp input is linearly proportional to V_{in} . Thus, the transition voltages can be estimated from the corresponding code densities and from these estimates, an estimate of INL_k as given in (2) can be expressed as

$$INL_k \cong \overline{INL}_k = \frac{H_k - H_1}{H_{N-1} - H_1} (N-2) - (k-1), \quad k = 1, 2, \dots, N-1 \quad (3)$$

Tests using $\overline{INL_k}$ as the measured value of INL_k are often termed histogram based tests and the histogram-based method is widely used to test ADCs.

3. Deterministic Dynamic Element Matching

In this section, we will first briefly review the DAC structure that DDEM is applied to. Then the Cyclic DDEM sequence approach is described and its performance when applied to a DAC is evaluated.

The proposed DDEM approach will be explained using a 3-bit current steering thermometer-coded DAC as shown in Figure 1.

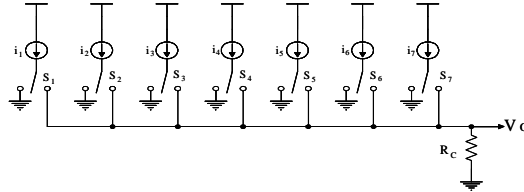


Figure 1: A 3-bit current mode thermometer-coded DAC

In this case, when all switches are connected to ground, the output corresponds to the digital word zero. To generate the output voltage for the digital 1, one switch needs to be connected to the output node. For a digital “k”, any k of the switches needs to be connected to the output node. The resistor R_C is picked so that when all of the currents sources are on, the voltage output is at the desired maximum.

The conventional random dynamic element matching idea for generating an output for a digital word “k” is to pick the location of k switches randomly each time an output corresponding to k is desired and then turn on those k switches. We can have multiple outputs for each digital word ‘k’ with different randomly selected current sources.

The proposed deterministic method picks the current sources to be switched deterministically. The pattern used attempts to distribute the sources to be switched on in a way that all sources are used almost statically uniformly. For simplification, one more current source element has been added to the DAC in Figure 1 such that the DAC has totally $N = 2^n$ current sources. The integer q is defined by the expression $q = N/p$ where it is assumed p, the number of samples per DAC input code, is selected such that q is an integer.

Both the RDEM and DDEM approaches take advantage of the fact that, for the INL calculation, the ADC needs to be tested from the static viewpoint, where the output of a DAC is used as the input to the ADC. The DAC’s output for the same input digital word, using different randomly or deterministically chosen current sources, will be input to the ADC p times. The ADC’s outputs corresponding to each one of the p input samples are then stored for calculating the INL later. In this way, the real-time limitations are eliminated, and a statistically linear input signal can be generated.

The DDEM approach will be described and its performance will be evaluated theoretically and verified by both simulation results and experimental results in the following sections. It will be also shown that DDEM outperforms RDEM in two aspects. One is that DDEM requires simpler control logic than RDEM for implementation, and the other is that ADC test based on DDEM is more accurate than that based on RDEM for the same given p.

3.1 Cyclic DDEM Switching Sequence

In this subsection, we will describe a Cyclic DDEM Sequence that gives reasonably performance and implementation simplicity. The current sources are arranged conceptually and sequentially around a circle, as seen in Figure 2, to visualize a wrapping effect whereby the N^{th} current source is adjacent to the first current source. In Figure 2 example, $k = 5$, $n = 4$, $N = 16$, $p = 4$, and $q = 4$. The physical layout of the current sources need not have any geometric association with this cyclic visualization.

We will denote p current sources as index current sources by the sequence $I_1, I_{1+q}, I_{1+2q}, \dots, I_{1+(p-1)q}$. These index current sources are uniformly spaced around the circle. For each input code k, $1 \leq k \leq N$, the DAC generates p output voltages. Each output voltage is obtained by switching k current sources consecutively starting with one of the p index current sources. Thus, the d^{th} sample ($1 \leq d \leq p$) is obtained by switching k current sources starting with $I_{1+(d-1)q}$ and continuing around the circle in the clock-wise direction until exactly k current sources have been selected.

We will term this the Cyclic DDEM Switching Sequence. It may appear to be similar to some of the DDFN approaches that are in use but, in contrast to the DDFN approaches, the Cyclic DDEM Switching Sequence is not data dependent and is completely deterministic.

At this point, a comparison between the Cyclic DDEM Switching Sequence and the random DEM switching sequence can be made from a hardware implementation viewpoint. It can be shown that the logic needed to implement the Cyclic DDEM approach is much simpler than that needed for a completely random DEM switching sequence. No scrambler is needed in the Cyclic DDEM approach and since the index current source values are shifted by a fixed amount, a shift register can be used to drive the switches that select the current sources.

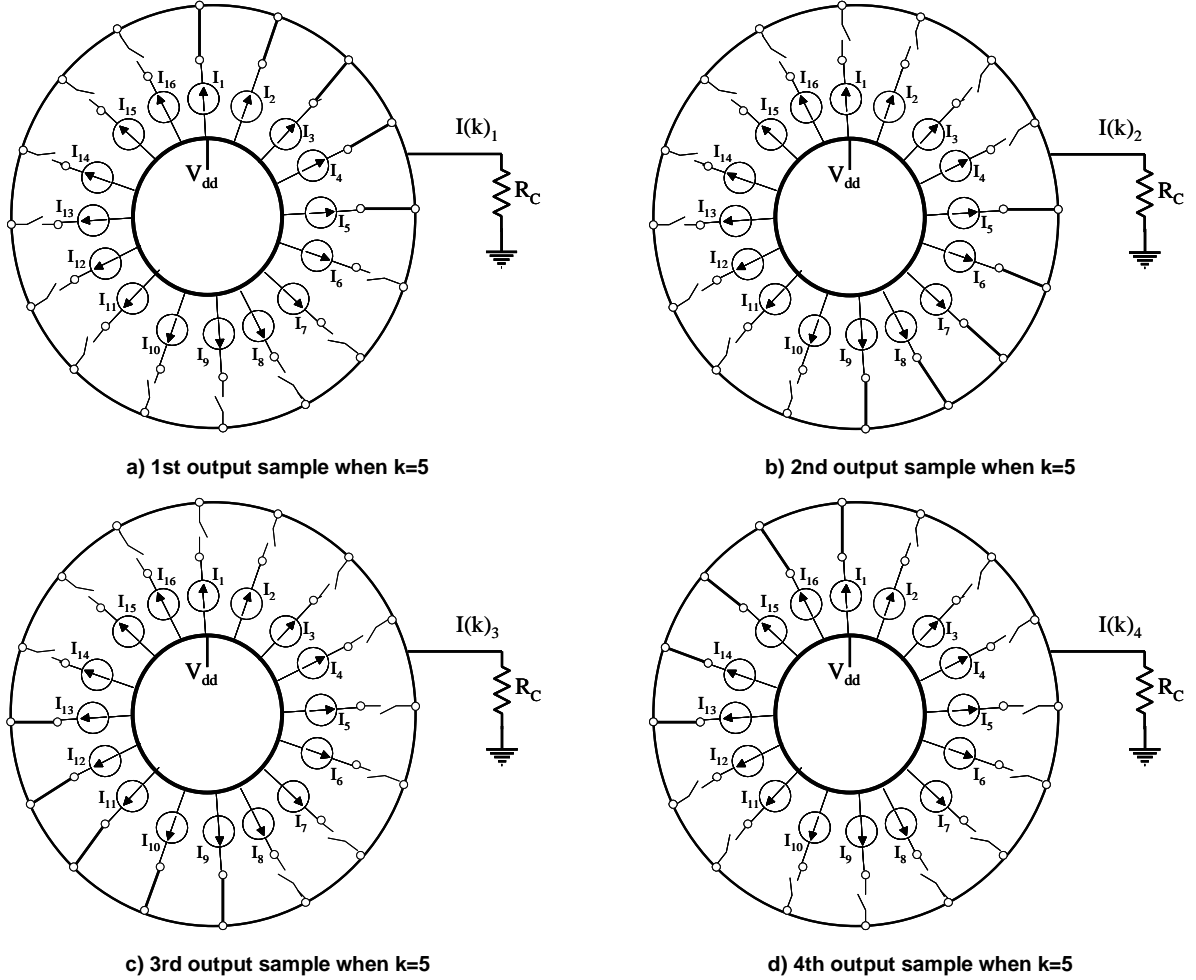


Figure 2: Cyclic DDEM switching of a 4-bit DAC

3.2 Performance evaluation of the deterministic DEM switched DAC

For each input code k , the DAC outputs p samples. Each output is the summation of the selected k current elements (scaled by R_c). The d^{th} current summation is denoted by $I_d(k)$. We have

$$I_d(k) = \sum_{j=1}^k I_{(d-1)q+j} \quad d = 1, \dots, p \quad (4)$$

The average of p samples is denoted by $\bar{I}(k)$

$$\bar{I}(k) = \frac{1}{p} \sum_{d=1}^p \sum_{j=1}^k I_{(d-1)q+j} \quad (5)$$

The statistical performance of the DAC output will be evaluated based on $I_d(k)$ and $\bar{I}(k)$. Suppose that the designed value of all current elements is I_0 . Due to process and other variations, the actual value of each current source is given by:

$$I_j = I_0(1 + \varepsilon_j) \quad (j=1, \dots, N) \quad (6)$$

We assume ε_j *i.i.d.* $\sim N(0, \sigma^2)$ where σ^2 is determined by design and process variations.

The overall output range is determined by $I(N) = N \cdot I_0 + I_0 \sum_{j=1}^N \varepsilon_j$. The nominal output range is $N \cdot I_0$. However, due to variations, the actual output range may not reach the nominal value. To make sure that DAC output range covers the DUT input range, we must guarantee the DAC nominal output range to be larger than the ADC input range.

We will first inspect the average of the p output samples for each DAC input code k . To evaluate the linearity of the averaged output, we define an end-point fit line which connects $(0, I(0))$ and $(N, I(N))$. When $k = t \cdot q + s$ ($s=1, \dots, q$, $t=0, \dots, p-1$), it can be shown that the expected values of all the averaged output current $\bar{I}(k)$'s are on the fit line, and the standard deviation is given by

$$\sqrt{\frac{q(q-s)}{4pq}} \sigma \cdot I_0 \quad (7)$$

If $n=16$, $p=64$ and $\sigma=0.1$, the maximum normalized standard deviation of the $\bar{I}(k)$'s is only 0.2, which shows that averaged output is almost uniformly distributed.

All the p output samples for code k center at $\bar{I}(k)$, and approximately obey the Gaussian distribution

$$N\left(\bar{I}(k), \frac{(N-k)k}{N} \sigma^2 \cdot I_0^2\right) \quad (8)$$

With proper approximation, when p is large, all the output samples of the DDEM DAC obey a distribution with the following PDF.

$$f(x) = \sum_{k=1}^N f(x|k) \cdot P(k) \quad (9)$$

Here, $f(x|k)$ is the PDF corresponding to (8) and $P(k)$ is the probability of each input code k . $P(k)=1/N$. For a DAC with given number of bit, p and σ are the two key parameters to determine equation (9). Though equation (9) is too complicated to simplify mathematically, we can draw the overall PDF as a combination of Gaussian PDF's with the aid of MATLAB. Figure 3 depicts the output PDF of a 10bit DDEM DAC. For this example, σ is chosen to be 0.1 and p is set to 64. From this figure, the output PDF is very flat except near the end points. Actually, near the end points, due to the small variances which can be calculated from (8), the PDF is discontinuous and fluctuates. The histogram of a DAC is a realization of such PDF, and must also be uniform except near the end points.

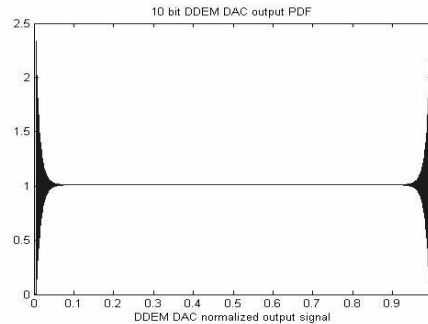


Figure 3: Output PDF of 10 bit DDEM DAC

The flatness of the PDF comes from two essential facts. One is that the averaged value $\bar{I}(k)$ which is the center of the individual distribution for each code k is almost uniformly distributed, and the other fact is that all the individual distributions for each code k have proper variances such that the combined distribution is continuous and flat. From equation (7), we can see that larger p leads to smaller variances for $\bar{I}(k)$'s and hence makes the distribution of $\bar{I}(k)$'s more uniform. Furthermore, increasing p means increasing the number of total output samples. Larger sample number will definitely make the shape of histogram closer to the flat shape of PDF statistically. In a word, large p helps to achieve a uniform histogram.

4. DDEM testing simulation results

To verify the DDEM approach, we simulated testing flash ADCs with resistor mismatching by using a DDEM DAC with lower resolution/accuracy than the ADCs. In simulation, the DDEM technique is applied to a simulated current mode thermometer-coded DDEM DAC with static mismatching error in the current sources.

Most existing ADC testing approaches utilize DACs that have higher resolution than the DUT. This is generally considered necessary to avoid the introduction of significant quantization errors. Since the statistical linearity of the DDEM DAC can far exceeds its resolution, the question of whether the DDEM DAC resolution can be reduced to levels comparable to or possibly even less than the resolution of the DUT deserves attention. We will not provide a detailed investigation of this issue in this paper but will consider the specific situation where the resolution of the DDEM DAC is less than that of the DUT. Specifically, an 8-bit resolution DAC with 3 LSB INL was used to test 1000 12-bit and 11-bit ADCs with $p=256$. The DAC has current sources mismatch modeled by a Gaussian distribution with $\sigma = 0.3$ and truncated on the 50% variation. The Flash ADC resistor strings are generated in a similar manner with $\sigma = 0.15$.

The simulation results are depicted Figure 4 and Figure 5. The INL_k plot of the original DAC without DDEM is shown in Figure 4. In Figure 5 (a) and (b), the INL_k testing errors using the DDEM DAC with different p for an 11-bit ADC and a 12-bit ADC are depicted respectively. For the 11-bit ADCs, the average maximum INL_k error was 0.65 LSB with $p=256$, while for the 12-bit ADCs was 1.52 LSB with $p=256$. It should be pointed out that if an ideal 8-bit DAC is used to test the 12-bit ADCs, the average maximum INL_k error is equal to 16.5 LSB.

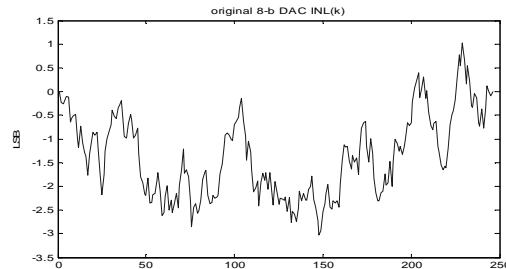
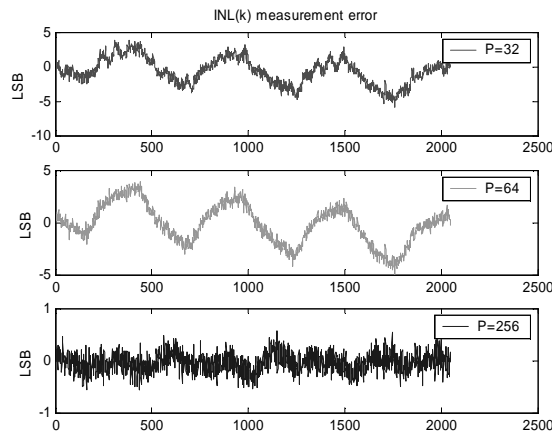
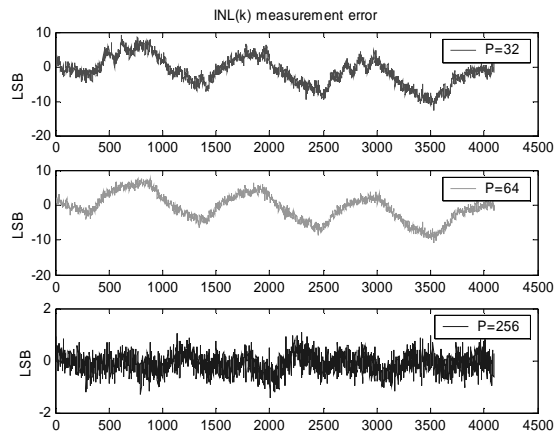


Figure 4: INL_k of the original DAC.



(a) INL_k test error for 11-bit ADC



(b) INL_k test error for 12-bit ADC

Figure 5: INL_k test error with varying p

From these results we can go even further by increasing the DAC resolution to test high resolution ADCs. Figure 6 shows the simulation results obtained when a 14-bit DAC is used to test 16-bit ADCs with $p = 256$. The DAC INL without using DDEM is 17.2 LSB, so the DAC linearity is 10 bits. The figure depicts the estimated ADC INL's versus their true INL's. We can appreciate how the estimated INL is always bigger than the real INL, which means that no bad parts will be sent to the customer.

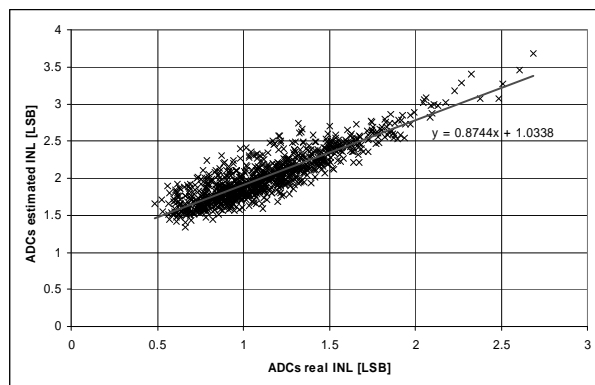


Figure 6: ADCs real INL vs ADCs estimated INL

It was mentioned in the previous section that deterministic DEM outperforms random DEM in implementation simplicity. A direct comparison of RDEM and DDEM for testing ADCs was also made in simulation. In Figure 7 we compare the performance of estimating the INL's of 100 7-bit ADCs using RDEM and DDEM respectively with $p=128$. In the comparison, the same 10-bit DAC with an INL of 10.1 LSB was used. From Figures 7, one important observation can be made that the DDEM method offers substantial improvements in performance over that of the random DEM approach for a given number of samples.

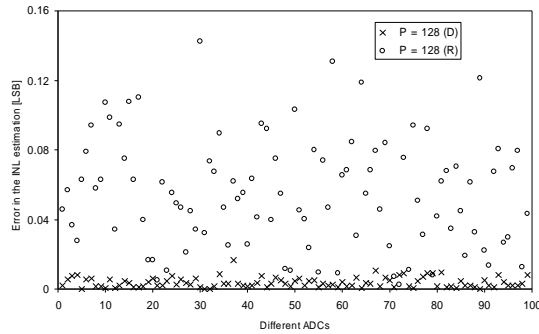


Figure 7: Comparison of RDEM and DDEM for estimating 100 ADCs' INL with $p=128$

5. DDEM DAC design and experimental results

To validate the DDEM approach further, an 8-bit DDEM DAC was designed and tested. In this section, we will first talk about some issues about the DDEM DAC design and then provide the measurement results.

5.1 DDEM DAC design

To implement the DDEM DAC, two critical parts of the design are the current source element and the DDEM control logic circuit. Other design issues such as gradient effect and output nonlinearity should also be considered. Benefited from the DDEM approach, the design is a quick and simple design, and the DAC occupies very small die area.

a) Current source element

There are quite a few current steering DAC structures. Since with the DDEM approach, the element matching issue is not critical, we can use a simple structure which uses fewer devices and hence less die area. Also DDEM makes it possible to use small-sized devices. By using a simple structure with small-sized devices, the DAC speed can be very high since it has small parasitic and therefore small capacitance load.

The current element structure used is the simple single-supply positive-output structure with three PMOS transistors [29] as depicted in Figure 8. To balance the output, both M1 and M2 have their drains connected to an output resistor respectively. We have $V_u > V_b > V_d$, and one shifter register unit (SR) to control M2's gate. If the M2's gate is connected to V_u , the current in this current unit flows through M1 and R_p to the ground, and if M2's gate is connected to V_d , the current flows through M2 and R_n to the ground. For the single ended output mode, the voltage crossing either R_p or R_n serves as the output voltage. And for the differential output mode, the voltage difference between R_p and R_n serves as the output.

To maximize the speed, the reference voltages should be chosen properly such that during switching none of the transistors will go into deep saturation or deep triode region.

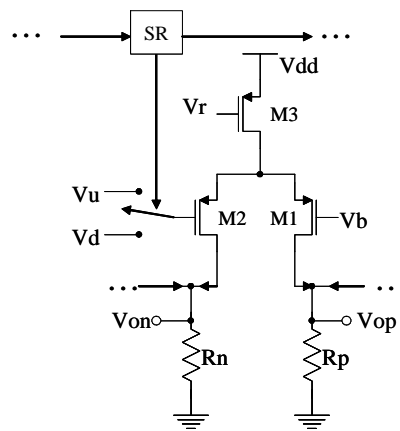


Figure 8: Current steering element structure

b) DDEM control logic

The control logic circuit is just a 256-bit shift register ring with each unit controlling one current source element. Starting from the all-zero state, one of the register units is selected as the starting point and a logic ‘1’ is continuously pumped into this unit. Then each time the clock signal advance, one more register unit is set to ‘1’. Thus the DAC output a monotonic ramp voltage by cluster current on R_p . In the meantime, the voltage crossing R_n is a declining signal. When all register units are set to “1”, one RESET signal clears all the units, a different start point is chosen and the same operation is applied. To achieve high speed with small die area, the simple shift register was adopted as shown in Figure 9. It contains only 6 transistors with 2 CMOS inverter and 2 NMOS transistor switches in series. Two-phase non-overlapping clock signals are required to drive this shift register. [30]

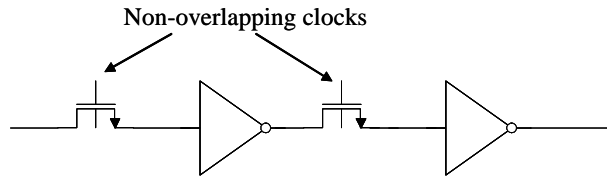
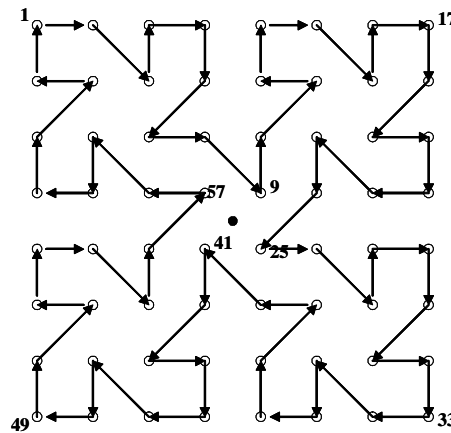


Figure 9: 6-Transistor shift register unit

d) Layout strategy

The random mismatching error between current elements can be averaged out by DDEM. However, the overall gradient effect on the chip die can not be cancelled by DDEM. The following layout scheme is used in design to cancel the gradient effect. Figure 10 depicts a 6-bit DDEM DAC layout scheme as an example. The circles in Figure 10 represent the current source elements in a chain. For any possible p , the selected starting points share the same common central node (the black dot on the central of the layout) and therefore the current elements switched for each DAC input code k share the same common central node under DDEM. For example, when $p=4$, the 4 starting points are the four elements numbered as 1, 17, 33 and 49 that center at the black dot. Hence the overall linear gradient effect can be cancelled with this layout strategy.



Each ○ represents one current source element +shifter register

Figure 10: Layout scheme of a 6-bit DDEM DAC

d) Output nonlinearity compensation

Due to the nonlinearity of the devices, the output voltage (say, the voltage across R_p) may have nonlinear error in it. This nonlinear error can not be cancelled by DDEM. To achieve high test accuracy, this nonlinearity should be minimized through proper design and layout.

5.2 Measurement results

The 8-bit DDEM DAC was fabricated in MOSIS AMI 0.50 μ m standard CMOS process. The core die size is about 0.9mm \times 0.9mm for double 8-bit DACs (0.4 mm² for each single DAC). The die photo is shown in Figure 11. The power supply voltages are 5V for both digital and analog parts. The power consumption is 260mW for the analog part and 60mW for the digital part with 0~1V output range at single ended output node (-1~+1V for differential mode).

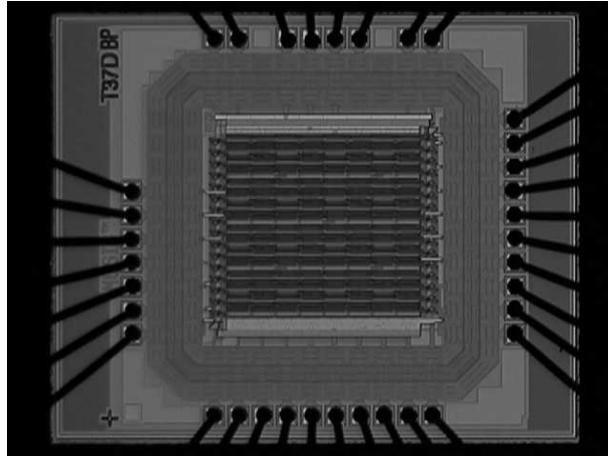


Figure 11: Photo of the DDEM DAC die

To test the DDEM DAC performance, DDEM control signals generated by a pattern generator were applied to the DAC and the DAC output (single ended mode) is sampled using a data acquisition board with high resolution ADCs. Though the DAC can operate at a speed of 10Msample/sec, the DAC was tested with a clock speed of 1 kHz due to the speed limitation by the data acquisition board. The DAC output with different iteration parameter p was collected and stored in computer for performance evaluation.

Figure 12 shows that without DDEM, the original 8-bit DAC has an INL error of 10.3LSB, which means the original DAC has a linearity of less than 5 bits. The main error source for this DAC is the output node nonlinearity. We can estimate the nonlinear error by measuring one or several samples from the fabricated chips. We can then apply the same nonlinear error compensation to all the chips from the same run.

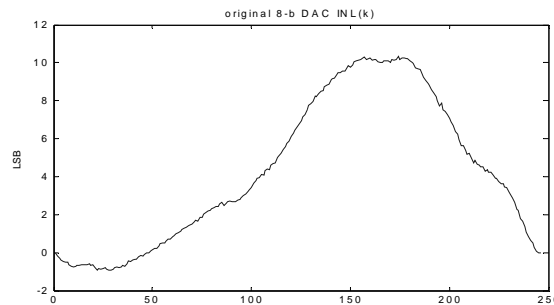
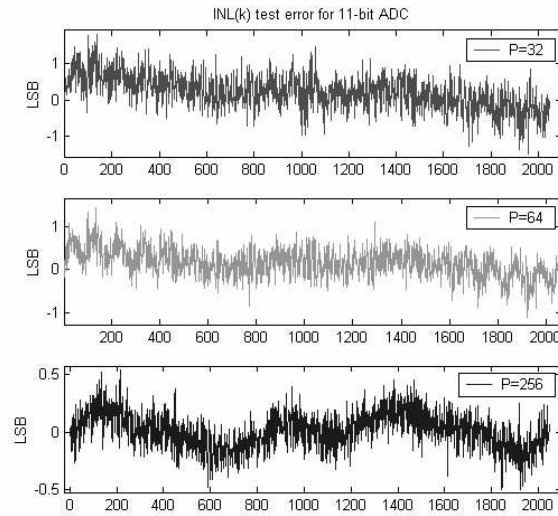
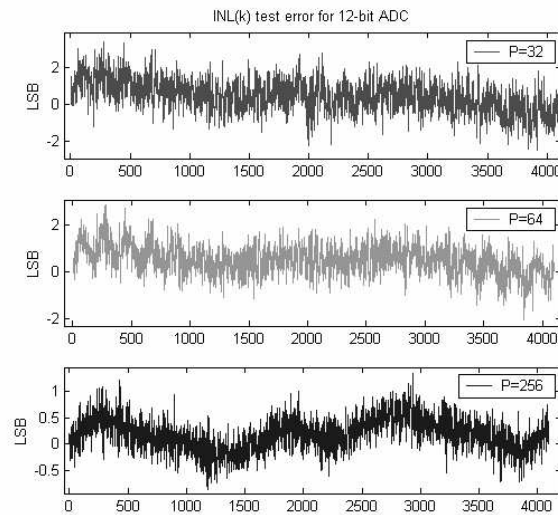


Figure 12: INL_k of the original 8-bit DAC



(a) INL_k test error for 11-bit ADC



(b) INL_k test error for 12-bit ADC

Figure 13: INL_k test error with varying p

The measured and stored DAC output was used as the stimulus to simulated ADCs and the ADCs' INL_k are estimated from the ADC output histogram. The simulated ADC's true INL_k are well known by calculation. We calculated the difference between the estimated INL_k and the true INL_k . The difference is just the test error with DDEM DAC output as the stimulus to ADC under test. To compensate for the nonlinear error, we first estimate the nonlinear error by testing one randomly selected DAC. Based on the estimated nonlinear error, we obtained the compensation values for testing ADC. Then the compensation values were applied to other DACs. Figure 13 (a) and (b) show the test errors after nonlinear error compensation for an 11-bit ADC and a 12-bit ADC with $p=32, 64, 256$ respectively. The simulated ADCs' INL ranges from 5LSB to 10LSB. From Figure 13 we can see that 1) the test error decreases dramatically when p increases; 2) when $p=256$ (full DDEM), the 8-bit DAC can test the 11-bit and 12-bit ADCs with error bounded by about ± 0.5 LSB and ± 1 LSB respectively using DDEM. (For the 12-bit ADC, the output histogram has around 32 hits for each bin.) Note such test performance is only achievable by using a DAC at least 12~13-bit linear if DDEM is not used, while in this case the original DAC's linearity is less than 8 bits without DDEM. It should be also noted that if the output node linearity is addressed then the error caused by current sources mismatches is eliminated by the DDEM, allowing us to use minimum sized devices.

6. Conclusions

In this paper a DDEM approach which is applied to low resolution/accuracy DACs for testing high resolution ADCs is described, characterized mathematically and also validated through simulation and experimental results. It was shown that with this approach DACs' linearity can be significantly improved statistically, and so DACs that are substantially less accurate than the ADCs under test can be used to generate the test signal for the ADCs. The DDEM is not used in the real-time signal path avoiding then some of the limitations related to using DEM for real-time signal processing. The proposed approach is also compared to a random DEM testing strategy showing that is substantially better than the standard random DEM approach from a testing viewpoint. An 8-bit current steering DAC with DDEM control was designed to verify the DDEM approach and its on-chip integrability. The measured and stored DDEM DAC output is used as stimulus to simulated ADCs under test. Experimental results clearly show that the testing error decreases when p increases. When $p=256$, the 8-bit DDEM DAC with original linearity less than 5 bits can be used to test 12-bit ADCs with test error bounded by ± 1 LSB. The DDEM DAC is capable of test high resolution ADC with satisfying accuracy. The technique offers potential for use both in BIST and production test environments, since the linearity of the testing signal generator is relaxed, and so the area required to implement it in silicon.

7. References

- [1] "2001 Edition International Technology Roadmap for Semiconductors," <http://public.itrs.net/Files/2001ITRS/Home.htm>.
- [2] M. Burns and G.W.Roberts, "An Introduction to Mixed-Signal IC Test and Measurement," Oxford University Press, New York, USA 2000.
- [3] K. L. Parthasarathy, Le Jin, D. Chen and R. L. Geiger, "A Modified Histogram Approach for Accurate Self-Characterization of Analog-to-Digital Converters", Proceedings of 2002 IEEE ISCAS, Arizona, May 2002.
- [4] J. Wang; E. Sanchez-Sinencio and F. Maloberti, "Very linear ramp-generators for high resolution ADC BIST and calibration" Proceedings of the 43rd IEEE MWSCAS, 2000, Volume: 2, 8-11 Aug. 2000 page(s): 908 -911 vol.2.
- [5] S. Bernard, F. Azais, Y. Bertrand and M. Renovell, "A high accuracy triangle-wave signal generator for on-chip ADC testing", The Seventh IEEE European Test Workshop Proceedings., 26-29 May 2002 Page(s): 89 -94.
- [6] B. Provost and E. Sanchez-Sinencio, "On-chip ramp generators for mixed-signal BIST and ADC self-test", IEEE Journal of Solid-State Circuits, Volume: 38 Issue: 2 , Feb. 2003 Page(s): 263 -273.
- [7] B. Dufort and G. W. Roberts, "Signal generation using periodic single and multi-bit sigma-delta modulated streams"; Proceedings 1997 International Test Conference, 1-6 Nov. 1997 Page(s): 396 -405.
- [8] M. F. Toner and G. W. Roberts, "A frequency response, harmonic distortion, and intermodulation distortion test for BIST of a sigma-delta ADC"; IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Volume: 43 Issue: 8, Aug. 1996 Page(s): 608 -613.
- [9] K. Arabi and B. Kaminska, "Oscillation built-in self test (OBIST) scheme for functional and structural testing of analog and mixed-signal integrated circuits"; Proceedings 1997 International Test Conference, 1-6 Nov 1997 Page(s): 786 -795.
- [10] F. Azaïz, S. Bernard, Y. Bertrand and M. Renovell, "Towards an ADC BIST scheme using the histogram test technique"; Proceedings 2000 IEEE European Test Workshop, 23-26 May 2000 Page(s): 53 -58
- [11] R. de Vries, T. Zwemstra, E.M.J.G. Bruls, P.P.L. Regtien, "Built-in self-test methodology for A/D converters"; Proceedings 1997 European Design and Test Conference, 17-20 March 1997 Page(s): 353 -358
- [12] Le Jin, K. L. Parthasarathy, D. Chen and R. L. Geiger, "A Blind Identification Approach to Digital Calibration of Analog-to-Digital Converters for Built-In-Self-Test", IEEE International Symposium on Circuits and Systems, Arizona, May 2002.
- [13] Le Jin, K. Parthasarathy, T. Kuyel, D. Chen and R. L. Geiger, "Linearity Testing of Precision Analog-to-Digital Converters Using Stationary Nonlinear Inputs", Proceedings 2003 International Test Conference, September. 2003.
- [14] K. Parthasarathy, T. Kuyel, D. Price, Le Jin, D. Chen and R. L. Geiger, "BIST and Production Testing of ADCs Using Imprecise Stimulus", ACM Transactions on Design Automation of Electronic Systems, October 2003.
- [15] R. J. Van De Plassche, "Dynamic element matching for high-accuracy monolithic D/A converters." IEEE Journal of Solid-State Circuits, Volume: 11 Issue: 6 , pp. 795 -800 Dec 1976.
- [16] L. R. Carley, "A noise-shaping coder topology for 15+ bit converters" IEEE Journal of Solid-State Circuits, Volume: 24 Issue: 2 , pp. 267 -273, April 1989
- [17] H. T. Jensen and I. Galton, "A Low-Complexity Dynamic Element Matching DAC for Direct Digital Synthesis." IEEE Transactions on Circuits and Systems, Vol. 45, pp. 13-27, January 1998.

- [18]H. T. Jensen and I. Galton, "An analysis of the partial randomization dynamic element matching technique" IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Volume: 45 Issue: 12, pp. 1538 -1549, December 1998.
- [19]B. H. Leung and S. Sutarja, "Multibit Σ - Δ A/D converter incorporating a novel class of dynamic element matching techniques"; IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Volume: 39 Issue: 1, pp. 35 -51, January 1992.
- [20]R. T. Baird and T. S. Fiez, "Linearity Enhancement of Multibit $\Delta\Sigma$ A/D and D/A Converters Using Data Weighted Averaging." IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing. Vol. 42, pp. 753-762, December 1995.
- [21]D. Cini, C. Samori and A. L. Lacaíta, "Double-index averaging: a novel technique for dynamic element matching in Σ - Δ A/D converters", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Volume: 46, Issue: 4, pp. 353 -358, April 1999.
- [22]R. E. Radke, A. Eshraghi and T. S. Fiez, "A 14-Bit Current-Mode $\Sigma\Delta$ DAC Based Upon Rotated Data Weighted Averaging." IEEE Journal of Solid-State Circuits. Vol. 35, pp. 1074- 1084, August 2000.
- [23]I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kotic, Jun Cao and Shu-Lap Chan; "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at $8\times$ oversampling ratio" IEEE Journal of Solid-State Circuits, Volume: 35 Issue: 12, pp. 1820 -1828, December 2000.
- [24]R. Adams et al, "Data-Directed Scrambler for Multi-bit Noise Shaping D/A Converters", US Patent 5,404,142, April 1995.
- [25]B. Olleta, D. Chen, and R. L. Geiger, "A Dynamic Element Matching Approach to ADC Testing". IEEE MWSCAS, Tulsa, 2002.
- [26]B. Olleta, L. Juffer, D. Chen, and R. L. Geiger, "A Deterministic Dynamic Element Approach to ADC Testing". IEEE ISCAS, Thailand, 2003.
- [27]H. Jiang, B. Olleta, D. Chen, and R. L. Geiger, "Parameter Optimization of Deterministic Dynamic Element Matching DACs for Accurate and Cost-Effective ADC Testing". IEEE ISCAS, Vancouver, 2004.
- [28]B. Olleta, H. Jiang, D. Chen, and R. L. Geiger, "Testing High Resolution ADCs using Deterministic Dynamic Element Matching". IEEE ISCAS, Vancouver, 2004.
- [29]D. A. Johns and K Martin, "Analog Integrated Circuit Design". John Wiley & Sons, Inc., 1997
- [30]J. M. Rabaey, "Digital Integrated Circuits: A Design Perspective". Prentice-Hall International, Inc., 1996