

Design for MOSIS Educational Program (Research)

**A Deterministic Dynamic Element Matching Approach
for Testing High Resolution ADCs Using Low Accuracy DACs**

Prepared by: Beatriz Olleta, Hanjun Jiang, Degang Chen and Randall L. Geiger

Institution: Dept. of Electrical and Computer Engineering, Iowa State University

Date of Submission: June 30 , 2003

Project description

Analog-to-Digital Converters (ADCs) are recognized as the world's largest volume mixed-signal circuit. With the increasing complexity of mixed-signal circuits and the emergence of low-cost mixed-signal IC market, testing of analog and mixed-signal circuits in general and ADCs in particular has become a challenging and costly process. Long test time and huge investment on commercial mixed-signal testers have resulted in the need for alternate testing strategies.

Built-in-self-test (BIST) structures offer potential solution not only in terms of reduction of costs associated with using testers, but also in terms of its ability to test deeply embedded systems on a chip (SOCs) and provide additional self-calibration facilities resulting in value addition of the parts. There have been many attempts in providing BIST solutions for ADCs, most existing approaches in the literature have been aimed at duplicating a standard tester on chip.

In the conventional approach to testing ADCs, a highly accurate signal is required to stimulate the device under test (DUT). This stimulus input is typically generated by a digital-to-analog converter (DAC) with substantially higher precision than that of the DUT. In duplicating the production testing approach, most existing BIST approaches also require signal generators that have substantially higher resolution and linearity than the DUT. This becomes a real challenge since such high performance signal generators require more design effort and more silicon area than the ADC to be tested.

Recently, we have developed a new philosophy for achieving analog and mixed-signal BIST. The basic idea of the new approach is to dramatically reduce the accuracy requirement on the signal generator but to use systems and signal processing techniques to accurately characterize and test the DUT. For this project, we will introduce a deterministic dynamic element matching (DDEM) technique for using low accuracy DACs to achieve very high accuracy in ADC testing.

In this work the deterministic DEM (DDEM) algorithm of current steering DACs for ADC testing was explained in detail with mathematical proof of its behavior. The DDEM approach is applied to the segment coded current steering DACs and the output of the DACs is used as the stimulus of the ADC under testing. In the proposed schemes, the DAC will have nominally more bits of resolution than the ADC but it is not ideal due to large static errors caused by mismatch. Static mismatch errors can be caused by process variations and result in a nonlinear transfer curve in the DAC for non-DEM DACs. However, the mathematical analysis shows that with the DDEM approach, the DAC can output analog signals that have evenly distribution and fine resolution which is very important for ADC testing.

The deterministic DEM method for testing ADCs was verified through simulations using Matlab. In the simulation, the DDEM approach was applied to 18-bit segment coded current steering DACs with low accuracy to generate analog signals for testing 16-bit ADCs and the ADC INLs were estimated using histogram testing method. The estimated INL was then compared to the true ADC INLs (in simulation we know the true INLs of the ADCs). Through simulations,, it was observed that the estimated INLs through the DDEM approach match the true ADC INLs very well and the estimation error is pretty small for by choosing proper DDEM parameters. It is also shown that the computation time required to testing one ADC is only several hundred milliseconds. The technique offers potential for use both in BIST and production test environments, since the linearity of the testing signal generator is relaxed, and so the area required to implement it in silicon.

To verify the performance of the DDEM approach, a 16-bit segment coded current steering DAC with DDEM control accessibility was designed and simulated in Cadence using the AMI05 process. The core part of the DAC occupies a chip area of about $0.8\text{mm} \times 0.8\text{mm} = 0.64\text{mm}^2$.

Fabrication process

AMIS C5F/N 0.50u

Packaging requirements

Standard 40 pin package, no specific requirement

Estimated project size

The design fits into one MOSIS TinyChip unit. Approximately 40 IO pins are required and the required area is 1.5 mm x 1.5 mm = 2.25mm².

Simulation plans

The DDEM approach was applied to the segment coded DAC structure. It is first simulated in Matlab, and the results obtained showed pretty good performance for ADC testing. A 16 bit segment coded (8 bit thermometer-coded+ 8 bit thermometer-coded) current steering DAC with DDEM control accessibility was then designed at the transistor level and simulated in Cadence. Since it is not computationally feasible to simulate the whole 16 bit DAC at the transistor level thoroughly, we simulated the whole 16 bit DAC for a few clock cycles. To verify the performance of the DDEM DAC we simulated a reduced version of the DAC, say, an 8 bit segment coded DAC with layout parasitic.

Test and characterization plans

Iowa State University has a state-of-the-art \$ 1 million instrumentation lab that was donated by Roy J. Carver, which will provide the testing environment for the DDEM DAC. We will first build the DDEM control circuit with FPGA to generate the DDEM control signals which will be applied to the DDEM DAC. The DAC output will be used as the stimulus for a 14 bit ADC under testing. The ADC testing result will then be compared to the testing results with the traditional expensive testing instruments.

Bibliography

- [1] B. Olleta, D. Chen, and R. L. Geiger, "A Dynamic Element Matching Approach to ADC Testing". *IEEE Midwest Symposium on Circuits and Systems*, Tulsa, 2002.
- [2] B. Olleta, L. Juffer, D. Chen, and R. L. Geiger, "A Deterministic Dynamic Element Approach to ADC Testing". *IEEE International Symposium on Circuits and Systems*, Thailand, 2003.
- [3] B. Olleta, H. Jiang, D. Chen and R. L. Geiger, "A Deterministic Dynamic Element Matching Approach for Testing High Resolution ADCs with Low Accuracy Excitations". *Draft sent to IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*. June, 2003.