

Real-time Conversion of Signals from Biological Recognition Events into Electrical Signals

Ben Zhao, Arifur Rahman, Kalle Levon

Polytechnic University
Department of Electrical and Computer Engineering
6 Metrotech Center
Brooklyn, NY 11201

Design #:	69037
Design name:	isfet2
Technology:	AMIS_ABN, lambda=0.8um
Fabricated on run:	T3CSAP (12/1/2003)
Layout size:	2100x2100 μm^2

Project Description

The objective of the project is to develop a hybrid bio-molecular system, using floating gate Ion Sensitive Field Effect Transistor (ISFET) that optimizes the interface between biological membrane or chemical sensor and a silicon circuitry for the accomplishment of dynamic, real-time conversion of biochemical signals of the recognition events into electrical signals.

Design

The design of the test chip consists of both n-type and p-type floating gate ISFETs. The n-type floating gate ISFET has a channel length of 4 μm and width of 40 μm , and the p-type floating gate ISFET has a channel length of 4 μm and width of 80 μm . The expected threshold voltage (V_t) for nFET is 2.47V and pFET is -2.37V. Table 1 shows the device parameters for the test chip. To improve the sensitivity of floating gate ISFET, it is desirable to connect the floating to a large Metal 2 (M2) opening for the deposition of sensing materials, as illustrated in Figure 1.

	W/L (μm)	Area Metal 2 opening (μm^2)	Antenna Ratio	V_t (V)	Estimated V_t	Yield
Dual-Gate NMOS	40/4	122500	765.625	2.47	Open-Circuit	0%
Dual-Gate NMOS	40/4	105000	656.25	2.47	Open-Circuit	0%
Dual-Gate PMOS	40/4	122500	765.625	-2.37	Short-Circuit	0%

Table 1: Device parameters for the test chip, fabricated through MOSIS AMI 1.6um technology. The antenna ratio is calculated taking into account the M2 opening, connected to the floating gate.

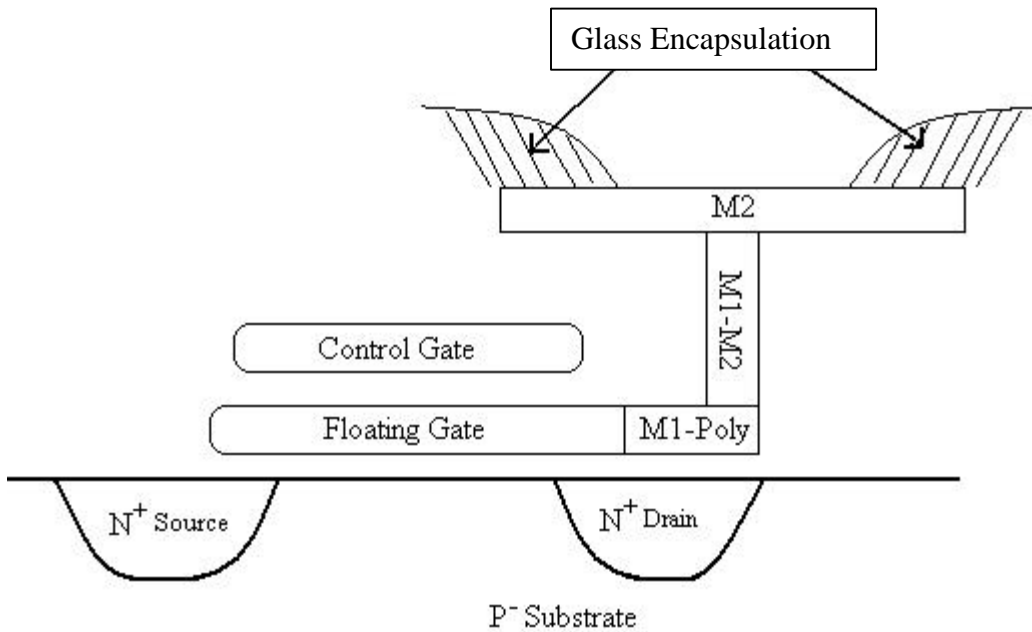


Figure 1: Cross sectional view of the n-type floating gate ISFET with M2 opening.

Analysis was performed to characterize the floating gate ISFETs. In n-type floating gate ISFETs, negative charges on the floating gate will induce positive charges on the channel. This results in n-type ISFETs devices having a higher threshold voltage (V_t). In our case, mostly likely significant amount of negative charges were accumulated on M2 opening, resulting in a large positive V_t shift. As a result, we were not able to turn on the device within acceptable range of power supply voltages. In p-type floating gate ISFETs, negative charges on the floating gate will induce positive charges on the channel. This resulted in the V_t being more positive for p-type ISFET. These mechanisms are shown on Figure 2 and 3.

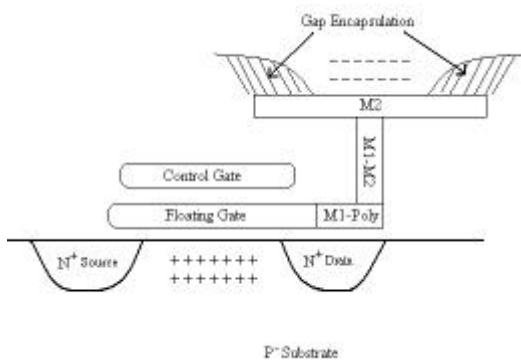


Figure 2: Cross sectional view of n-type floating gate, with negative charges on the M2 opening inducing positive charges in the channel. Resulting V_t is larger than expected.

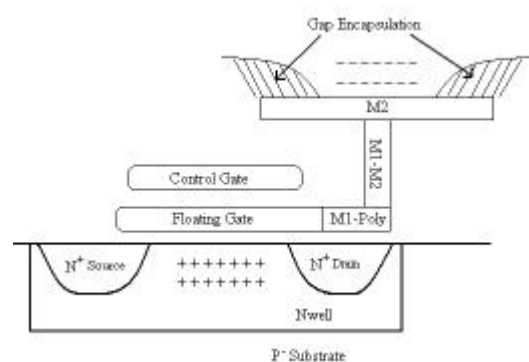


Figure 3: Cross sectional view of p-type floating gate, with negative charges on the M2 opening inducing positive charges in the channel. Resulting V_t is smaller than expected.

Measurements

Measurements were conducted on both the n-type and p-type floating gate ISFETs that were processed in AMI 1.6um CMOS technology. All pFETs measured were open-circuited and nFETs were all short-circuited. Figure 4 and 5 show the measured I_{DS} vs. V_{GS} for V_t extraction. Measurements of nFET devices show current within the noise limit, which can be explained by its high V_t , which is probably higher than 5 V. The pFET's V_t is approximately 0V.

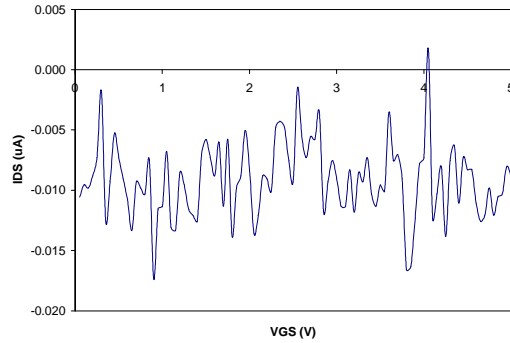


Figure 4: I_{DS} vs. V_{GS} curve of nFET device.

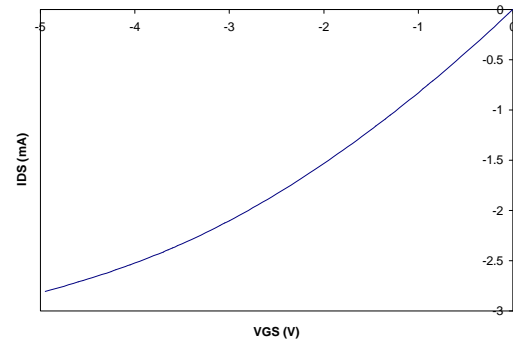


Figure 5: I_{DS} vs. V_{GS} curve of pFET device.

Analysis from different devices shows that the causes are related to the antenna design rule violation. Table 2 shows parameters of different devices with different antenna ratios. Devices with lower antenna ratio have higher yield.

	W/L (μm)	# Fingers	Area of Metal 2 Opening (μm^2)	Antenna Ratio	Calculated V_t (V)	Measured V_t (V)	Yield
Dual-Gate NFET	125.2/ 25.6	9	135000	4.68	2.09	1.1	50%-70%
Dual-Gate NFET	50/ 5.6	11	106000	34.41	3.45	3.1	<25%
Dual-Gate PFET	250/ 25.6	9	135000	2.34	-3.21	-2.7	50%-70%
Dual-Gate PFET	100/ 5.6	11	106000	17.20	-5.29	-4.1	<25%

Table 2: Device parameters from a previous batch of ISFETs, fabricated through MOSIS in AMI 1.6 um technology.

Experiment

Experiments were conducted with ISFETs using negatively doped aniline trimer in hydrochloric acid (HCl), which has the chemical structure shown in Figure 6, as a sensing material. It was injected onto the M2 opening and sensing was performed. Figure 7, shows the V_t shift due to the sensing of negatively doped trimer, deposited on the M2 opening an n-type ISFET. Due to the low-yield of ISFETs, we were not able to perform many experiments to screen sensing materials and characterize their sensitivity to gases or bacteria.

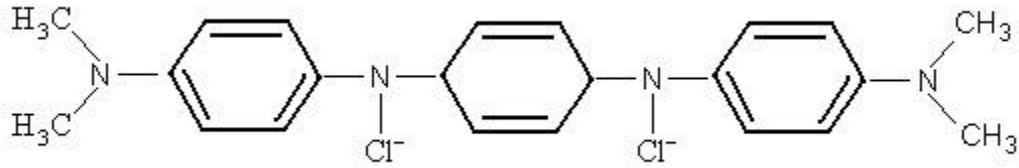


Figure 6: Structure of aniline trimer doped in HCl used for sensing.

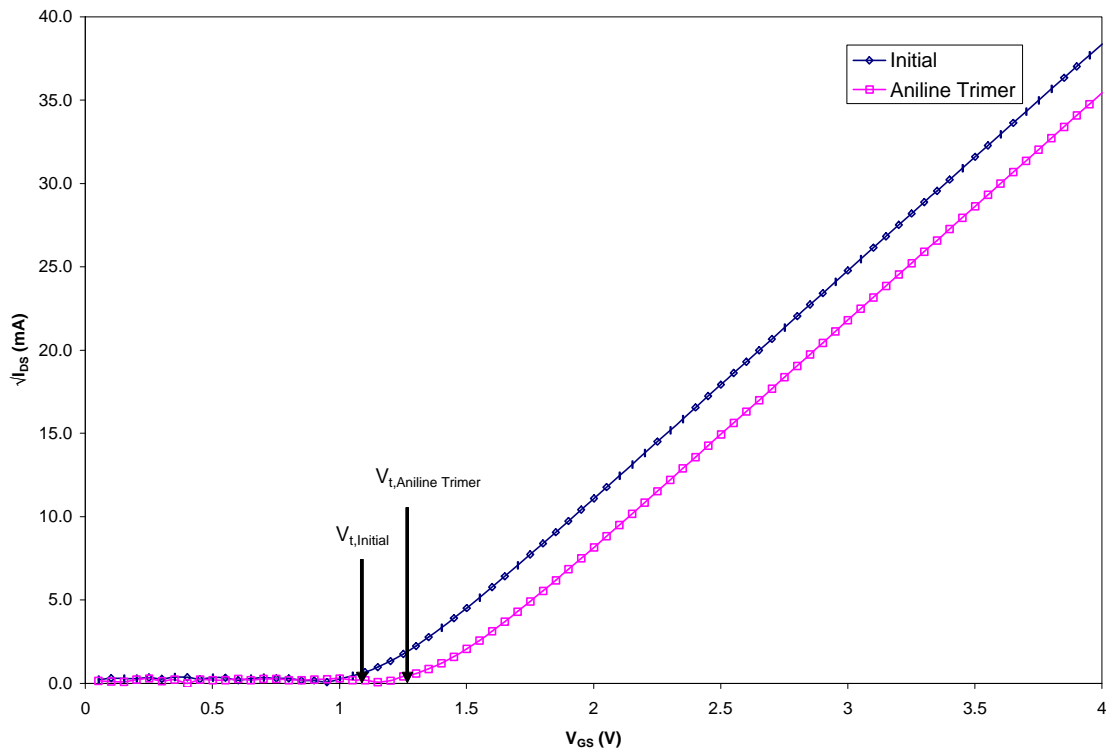


Figure 7: Initial $\sqrt{I_{DS}}$ vs. V_{GS} characteristics of a floating gate ISFETs and the same I-V characteristics after the floating gate is coated with aniline trimer. The ISFET is fabricated in standard $1.2\mu\text{m}$ CMOS process, available from MOSIS (www.mosis.org).

Summary

The test chip focuses on various antenna ratios and device dimensions to assess the dependencies of yield on device parameters. To achieve higher yield, there is a need to reduce antenna ratio, which also lowers the sensitivity of floating gate ISFETs. In future test chip designs, we will explore optimization of ISFET design by considering yield and sensitivity. An additional gate for injecting charges to or from the floating gate will be incorporated to optimize the V_t of ISFETs and to improve yield.

Acknowledgment

We would like to thank MOSIS for the ISFET test chip fabrication under MEP Research Program and their help in answering questions related to device design and fabrication.