

Ultra wide-band distributed CMOS Mixer (Broadband Receiver)

A Research/Educational Proposal

**Analog and Mixed-Signal Center (AMSC)
Department of Electrical Engineering
Texas A&M University
College Station, TX, 77840**

1. Goals of the Project

The author proposes a novel ultra wide-band distributed mixer that is a potential candidate of broadband system application. High frequency performance and ultra wide band performance are resulted with the implementations of distributed circuit concept.

This proposal addresses and wants to achieve the following goals:

- Exploration of the design methodology of distributed mixer in CMOS technology (Frequency from 3GHz-22GHz).
- Measurement methodology of high frequency circuit with on wafer probe testing.
- Preparation for the UWB system and broadband system design.

2. Background of the Applicants

Fan Xiaohua is currently Ph.D. students at the Analog and Mixed-Signal Center of Texas A&M University. His research is focused on the RF frond-end circuit design, distributed circuit design, and low voltage low power amplifier design.

2.1 Fabrication Process

The required fabrication process is TSMC 0.18 μm (CMO18) mixed signal/RF process using non-epitaxial wafers and with thicker top metal. Because the designed distributed works above 20GHz, high threshold voltage transistor and thicker metal are needed to achieve the target performance. The use of such technology is necessary for this high frequency mixer design.

2.2 Estimated area and packaging

The required chip area is $3\text{ mm} \times 3\text{ mm}$ (9 mm^2). A TQFP package OCP_LQFP44A with 44 pins will be used. Open package is required so that the on wafer probe station can used to measure the performance.

3. Project Description

The development of RF and wireless applications requires wider signal bandwidth and higher working frequency in the circuit design. Because of the inherent limitation of the CMOS transistor, which is most about the threshold voltage limitation and constant gain-bandwidth product limitation, novel circuits are required to satisfy the requirement of the wide-band RF and wireless system. The allocation of frequency from (3GHz-10GHz) by Federal Communications Commission (FCC) to unlicensed use booms the research and commercial activities in ultra wide-band system and circuit design.

Furthermore, the researches on the circuits that can work above 20GHz even higher are much more competitive.

The mixer is an important component in RF and wireless communication system. It converts the signal from the RF to IF. Operating in high frequency and with broader bandwidth are two critical requirements for the mixer that works in broadband system. To satisfy the requirement of broadband system, distributed mixer is explored and analyzed in this project. The distributed mixer has several signal paths from the input to the output. Based on the solution of Maxwell equation, It is easily found that the distributed mixer can improve the bandwidth performance without sacrificing the other performance.

The method and theory of designing the novel distributed mixer is proposed, analyzed and will be tested using the CMOS technology in this project. This distributed mixer uses the distributed circuit concept and works through 3GHz-22GHz.

The traditional Mixer circuit (single balanced structure) is as shown in Figure 1.

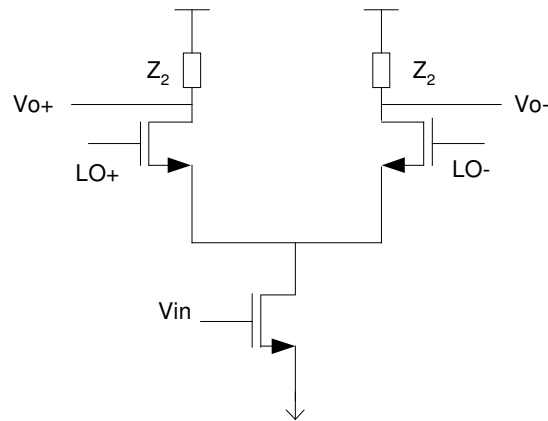


Figure 1. Transitional single balanced mixer

The mixer has three input signals: Vin, LO+ and LO- and two output signals: VO+, VO-. Because of the gain-bandwidth product is constant, It's difficult to design this circuit working in higher frequency above 20GHz without sacrifice the gain. Considering all five signals as distributed, we will get distributed mixer circuit as shown in Figure 2.

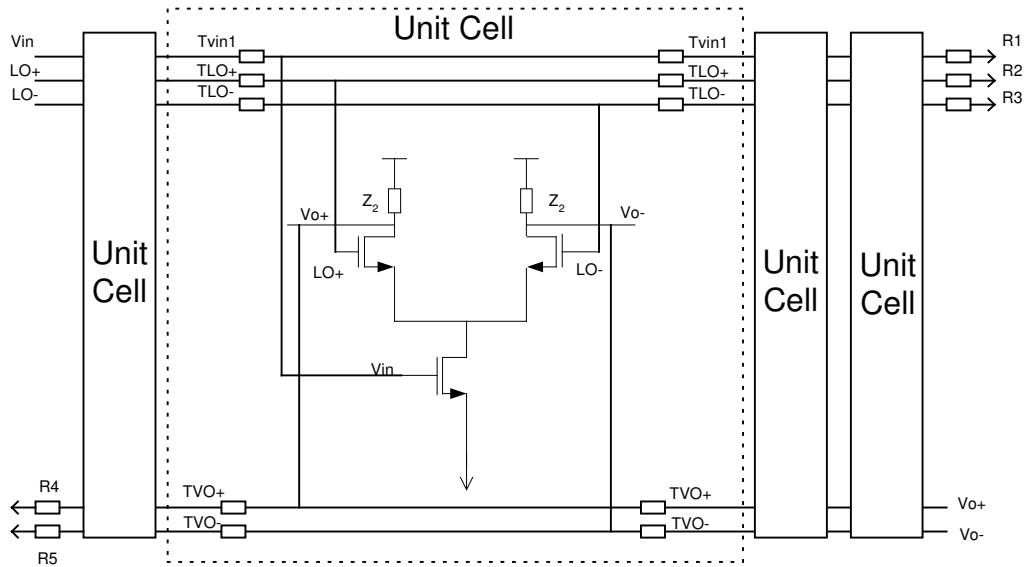


Figure 2. Distributed mixer topology

Based on this distributed concept, this mixer can work from 3GHz to 22GHz.

3.1 Simulation and Layout Plans

EM simulation software, IE3D HFSS and Sonata are used to simulation the transmission line. The transistor level design will be carried out using HP-ADS and SpectreRF. This will be done using SPICE model parameters provided by MOSIS for the TSMC CMOS 0.18 μ m technology and also using the transmission line model gotten from the EM simulation. The toolkit provided by MOSIS includes the model for cadence and also for HP-ADS, allowing the simulation of the circuits in two environments.

The layout of the final design will be created using the Virtuoso Environment of CADENCE™. Good layout techniques such as common-centroid and symmetric arrangements and dummy transistors should be used for better matching. In so high frequency region, the influence of the pads significantly deteriorates the chip performance. With the measurement results obtained by on wafer probe testing and calibration of the pad, the influence of the pads can be partly removed to have a better understanding of the proposed circuit.

3.2 Test Plans

The final stage will be the testing and characterization of the fabricated chip. On wafer probe is used to measure the conversion gain, noise figure and matching performance of mixer to remove the resistive and capacitive loading influence from the pads. A careful set up for measurement is needed. Towards this end open packaged die is required to do the on wafer probe testing. The dc bias would be provided via bonding wires from the PCB. A number of testing equipment are at our disposal: a Vector Network Analyzer (40 GHz): Agilent 8510C, Spectrum Analyzers (up to 40 GHz): Agilent 8562A and a frequency Synthesizer (40GHz): Agilent 83650L among testing equipment. We also have access to a high frequency Probe Station.

Students involved

Fan Xiaohua

Professor involved

Dr. Edgar Sanchez-Sinencio

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