

An Integrated Electronic Equalizer For Dispersion Compensation In 10Gb/s Fiber Networks (PROPOSAL)

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Abstract: This proposal presents the design of a high-speed transversal equalizer for dispersion compensation in 10Gb/s fiber networks. The seven tap equalizer has been implemented in a 47GHz SiGe technology. The equalizer circuit is optimized for minimum group delay and maximum bandwidth. We would like to apply for fabrication in a IBM 5HP SiGe processing via MOSIS MEP research program.

I. INTRODUCTION

Modal, chromatic and polarization mode dispersions are the major sources of transmission impairments in high data rate fiber communications. Without proper compensation, the performance of the fiber communication systems will be severely limited. The available dispersion compensation fiber is static in nature, and does not support agile optical networks. Other optical solutions are only capable of compensating one form of the dispersions with very high cost, high insertion loss and slow tuning speed if they are tunable at all. This project aims to build an adaptive electronic equalizer for the compensation of all forms of fiber dispersions. An electronic equalizer module is superior considering its cost, size, reliability, flexibility and speed. Our design is based upon a commonly used SiGe technology with $f_T=47\text{GHz}$ for 10Gb/s fiber networks and thus has the potential to be integrated in the whole receiver IC for cost reduction.

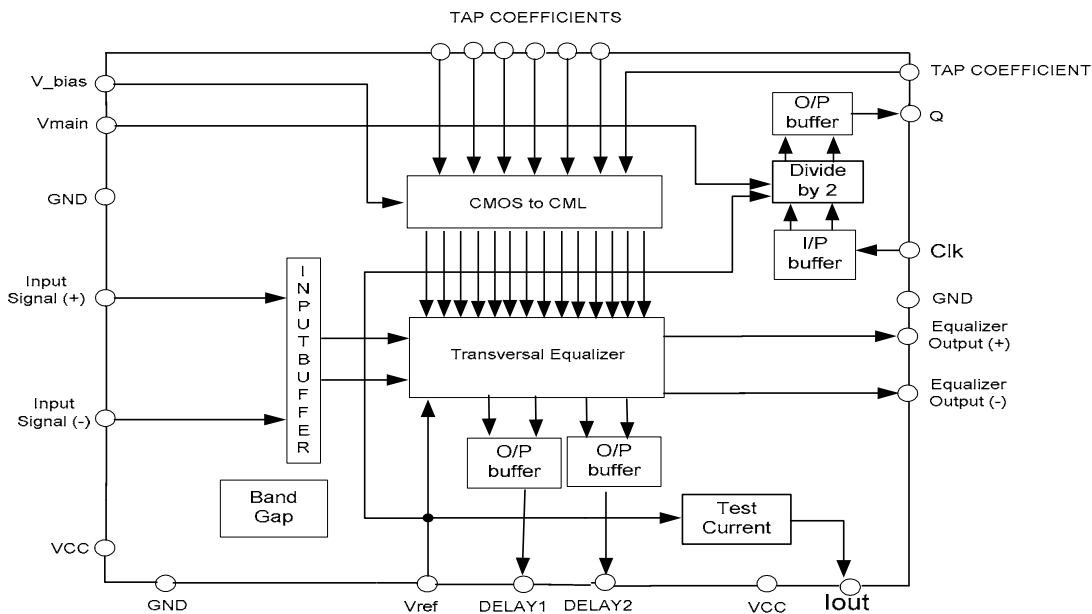


Fig.1. block diagram of the chip

II. Project Description

The proposed chip (fig.1) has an input buffer, and an transversal equalizer. The tap coefficients are given as inputs to the CMOS to CML converter and its output (differential) are fed as tap weights to the variable gain amplifiers in the transversal equalizer. The output's of the variable gain amplifier are added in current mode and will be tied to external pull-up resistors.

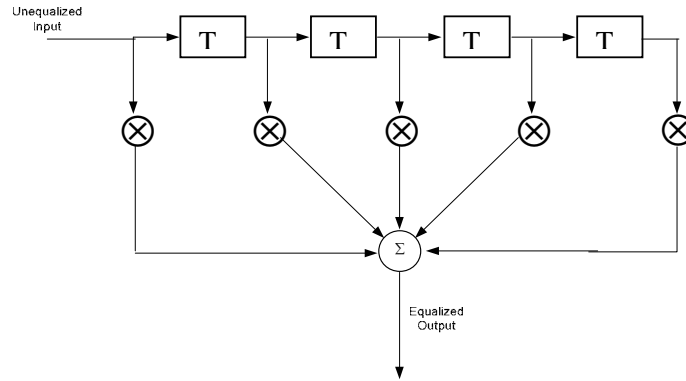


Figure 2 Linear transversal equalizer.

The linear transversal equalizer is essentially an tapped delay line. The delay elements are designed using unity gain amplifier and the tap weight is realized using variable gain amplifier.

Fig.3. shows the simulation of the gain and group delay of the delay cell and Fig.4. shows the gain and group delay of the variable gain amplifier.

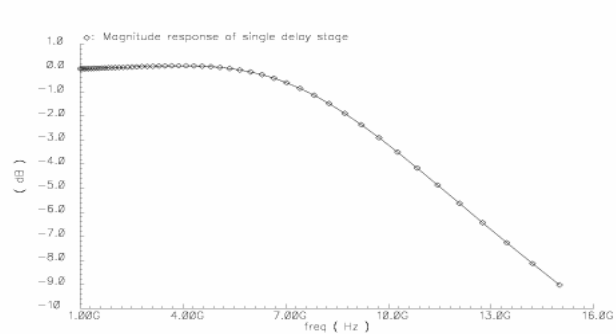


Figure 3 Magnitude response of the delay stage. The 3-dB frequency is at 10 GHz.

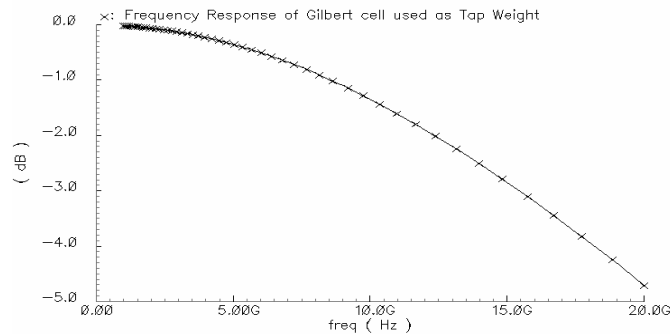


Figure 4 Phase response of the Gilbert variable gain amplifier

III. EQUALIZER SIMULATION RESULTS

A seven tap equalizer has been implemented in a 47 GHz SiGe technology. Fig.5.1-5.4 gives the simulated equalizer outputs with specified tap gains. It demonstrates that the equalizer circuit can implement various filter characteristics such as low pass, notch, bandpass and high pass. Thus, the equalizer is capable of constructing any inversed transfer functions of the dispersive channel for dispersion compensation by adapting zero's at various frequencies. T1~T7 are the 7 tap weights in the transversal equalizer.

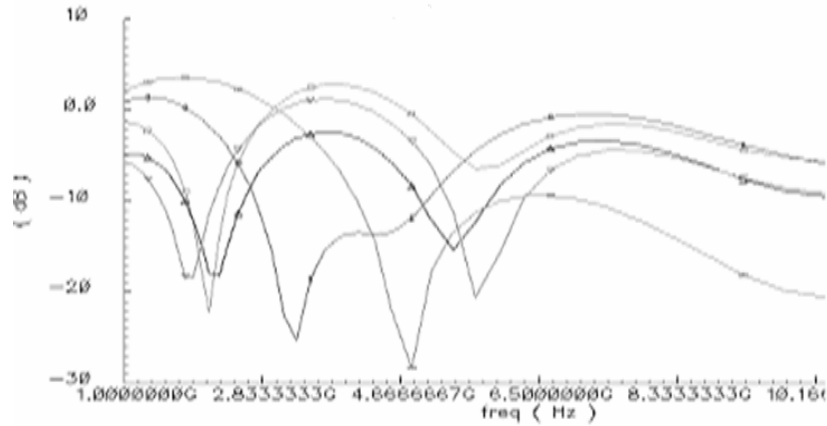


Figure 3.1 Simulated equalizer transfer function with zeros at various frequencies for different tap coefficients.

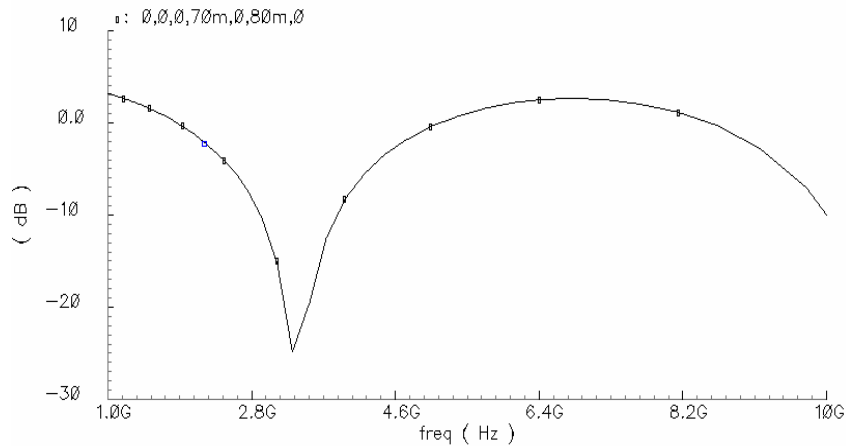


Figure 3.2 A notch filter implemented with tap inputs 30mv, 0, 0, -70mv, 0, 0, 50mv

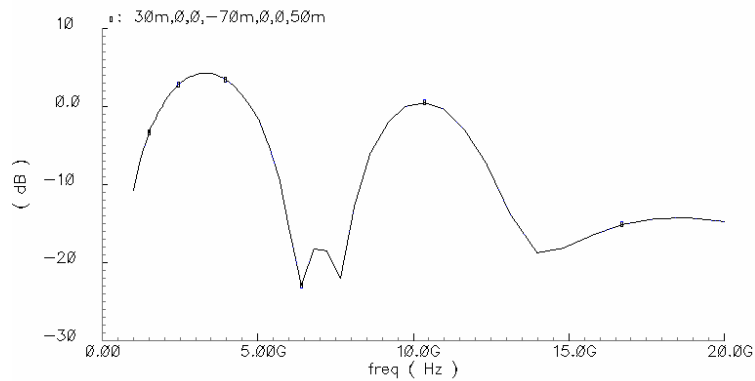


Figure 3.3 Band-Reject filter implemented with tap inputs 30mv, 0, 0, -70mv, 0, 0, 50mv

IV. PROJECT DETAILS

Estimated Project Size:

Being the result of recent theoretical research investigations, none of the above results are currently sponsored. We therefore ask for support of the following run:

- Process: SiGe 5HP [0.5 um].
- Estimated project size (length and width): 2.036 x 1.450 (layout size 1.880 x 1.263 mm²).
- Package size: 32 pin plastic package QFN32A (bonding diagram attached).
- Time: The project has been submitted to MOSIS with the following status.
- Project Status:

Design 71548 status: AWAITING QUOTE OR FUNDING
Design name: Auburn_TE
E-mail address: daifa01@eng.auburn.edu
Phone number: 334-844-1863
Technology: IBM_5HP
Fabrication restricted to IBM only.
This project can be fabricated on a IBM_5HP run using 5HP.
Layout format: GDS
Top or root structure is "top_V47_bk".
Layout file: complete; Binary CRC checksum: 1213606786,
7161856
Intended disposition: RESEARCH
Design Kit Version: V2.7.0.1
Bonding pads: 24
Layout size: 1880 x 1263 microns; area: 2.374 sq millimeters
Layers found: NS, NSONNW, DT, RX, NW, PB, RS, BB, BP, PDCON,
RP, CBAR, MCBAR, CEBAR, CABAR, M1, M1PIN, RN, V1, V1BAR,
M2, M2PIN, V2, V2BAR, LM, NU, DC, XN, BW, NE, N2, NP, LV,
Q2, PADFILTR, CHIPEDGE, FILLCELL, OLDEV, OUTLINE, BPERI,
DOC1, SUB
Requested quantity: 40
Requested packaging: QFN32A [waiting for your bonding diagram]
(30 parts), UNPACKAGED (10 parts)
Maximum die size: 2784 x 2784
A total of 40 parts are ordered
with 30 to be packaged in QFN32A
with 10 to be delivered unpackaged

Mosis-Reply-Id: 00113325-001-003

Simulation Plans:

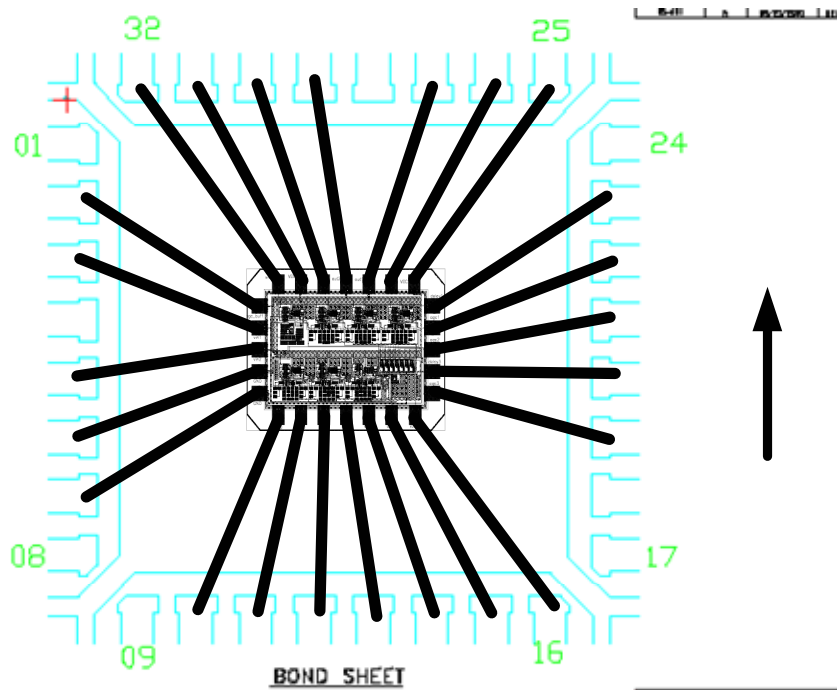
We have performed simulations using IBM 5HP lib under Cadence Analog Design Environment. The circuit pre-simulation is finished and the chip layout is pending. We expect complete the circuit design, layout and post-simulation by October21, 2004. We therefore request fabrication support on any IBM SiGe 5HP MPW shuttle runs starting from October25, 2004 through MOSIS.

Test and Characterization Plans:

We plan to perform chip testing at our department. The ECE department at Auburn is equipped with network analyzers, signal generator, spectrum analyzers, logic analyzers, digital oscilloscopes and wafer test probe station. For testing the dispersion compensation in a real fiber system, we need to rent Agilent 86100A DCA to monitor the optical eye patterns. The equalizer feedback system will be implemented in FPGA that provide the equalizer coefficient controls.

Bonding Diagram

Die Rotation (Clockwise) in package cavity: 0



- DESIGN_NUMBER:71548
- CUSTOMER-NAME: Foster Dai
- CUSTOMER-ACCOUNT:3823
- PHONE-NUMBER:334-844-1863
- FAX-NUMBER:334-844-1809
- QUANTITY-ORDERED:40
- QUANTITY-PACKAGED:30
- QUANTITY-UNPACKAGED:10
- PACKAGE-NAME:QFN32A
- PACKAGE-CAVITY-SIZE:2.78*2.78
- MIN-PAD-SIZE-X:110 micron (5HP requires min-pad-size 95 micron)
- MIN-PAD-SIZE-Y:110 micron (5HP requires min-pad-size 95 micron)
- MIN-PAD-PITCH:215 micron (5HP requires min-pitch 115 micron)
- DIE-ROTATION(CLOCKWISE)-IN-PACKAGE-CAVITY: 0

V. CONCLUSIONS

We have implemented a 10Gb/s high-speed analog equalizer with 7 taps in a low cost 47GHz SiGe technology. The designed equalizer MMIC is to be fabricated in a 47 GHz SiGe processing.

VI. REFERENCES

1. Vasanth Kakani and Foster F. Dai, "Integrated Electronic Equalizer for Dispersion Compensation in 10Gb/s Fiber Networks", *IEEE 5th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Atlanta, GA, September, 2004.
2. Vasanth Kakani, Foster F. Dai, and Richard C. Jaeger, "Delay Analysis and Optimal Biasing for High Speed Low Power CML Circuits", *IEEE International Symposium on Circuits and Systems (ISCAS)*, pp.869-872, Vancouver, Canada, May 2004.