

MOSIS Report for MEP Research Program, Research Account

A Transform CMOS Imager

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1. Introduction to the Transform Imager

This chip was designed to primarily test the performance of newly designed circuitry for a large scale CMOS transform imager. This chip has the ability to perform certain separable block transforms at the focal plane of the form:

$$Y = A^T P B \quad \text{Where } Y \text{ is the output,} \tag{1}$$

P is the acquired image, and
A,B are coefficient matrices

This operation allows for a large family of useful image processing related transformations to be performed. Among these transformations are high pass and low pass filters, edge enhancement, and DCT operations which are the basis of JPEG compression. This chip is a development over of previous work to develop the architecture of the transformation. The main goals of this chip were to test redesigned architecture and components for use in a large scale imager. Primarily interesting components here are the new input coefficient generation for matrix A, a redesigned pixel, and and redesigned readout circuitry component.

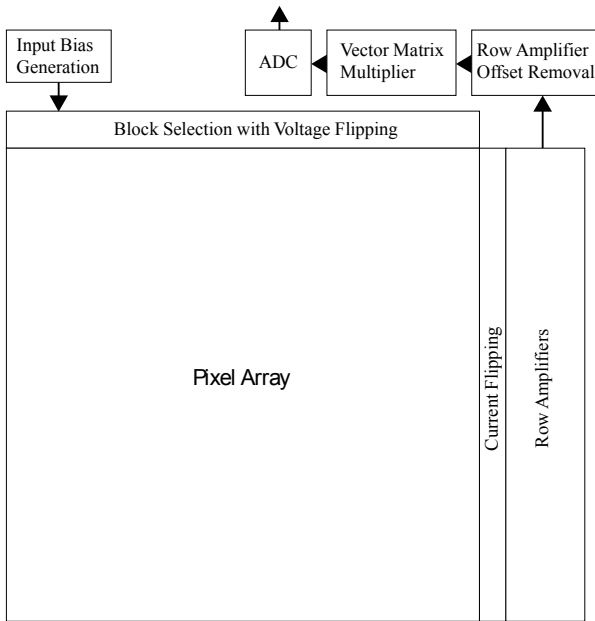


Figure 1.2.: Architecture Blocks



Figure 1.1.: Die photograph

2. Input Coefficient Generation

A key technology in the design of this particular approach for low power analog processing is the analog floating gate transistor. Similar to more common digital storage on EEPROM devices, an analog floating gate stores a charge on an insulated capacitor plate. Various methods for changing this charge have been developed which employ tunneling of electrons through the insulating material.

Figure 2.1 shows the basic design of a floating gate transistor element in a single poly process. To employ a floating node, polysilicon surrounded by silicon dioxide is used. Inputs at the input gate couple onto the floating gate to control the transistor. However, that input is given an offset determined by the amount of charge on the floating node. To vary this charge two techniques are used, Fowler-Nordheim tunneling and injection. The tunneling techniques involves placing a large voltages on the tunneling input to tunnel electrons off of the floating gate. The effect is seen in a gate sweep seen in Figure 2.2, where the effective gate voltage is raised (seen by a leftward curve shift) by the tunneling. On the other hand, injection involves turning the transistor on and using a large V_{ds} . This high field imparts carriers with high energy which through a process called impact ionization create electrons of high energy which reach the gate through the oxide, thus lowering charge. This effect is seen in Figure 2.3 where the curves are shifted to the right.

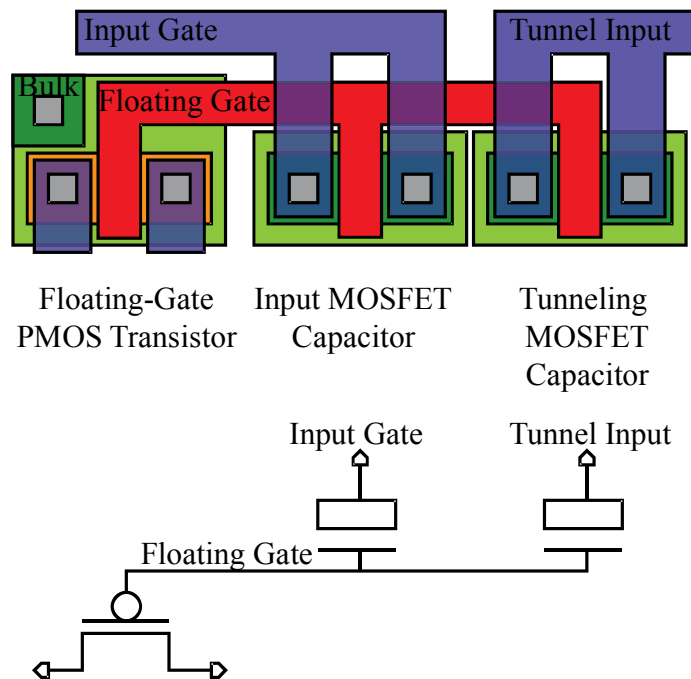


Figure 2.1.: Basic Structure of an analog floating gate transistor. A floating gate voltage serves to control the transistor which has a voltage determined by a stored capacitive charge and capacitively coupled voltages from the input gate and a tunneling input.

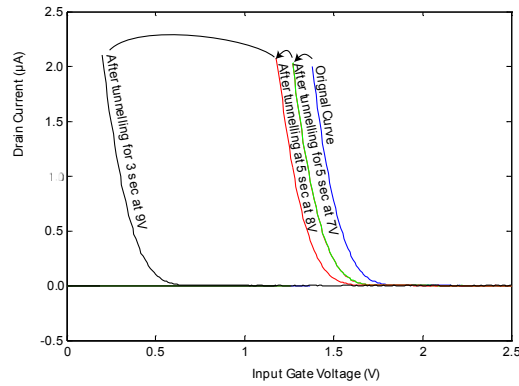


Figure 2.2: Using tunneling to raise the effective input voltage. With source and gate voltages at 2.5V, a curve initially lowered by 7V and 8V pulses finally moved significantly with a 9V pulse.

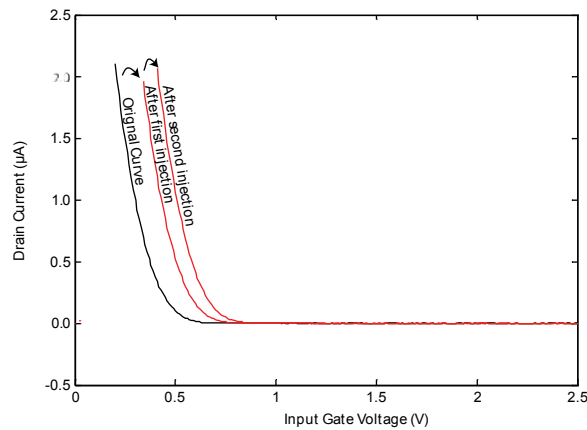
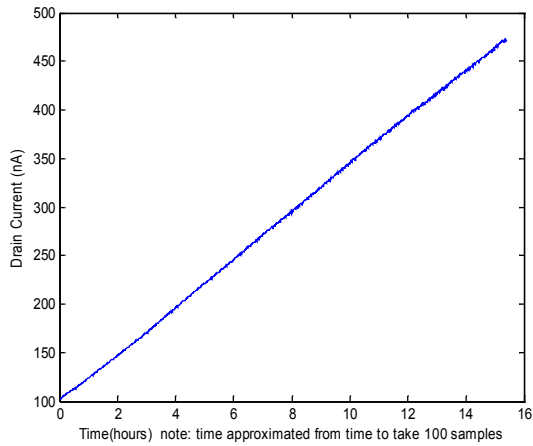


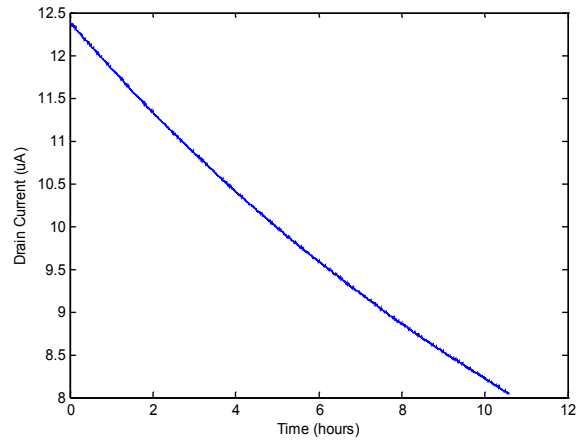
Figure 2.3.: Two successive injection pulses. The chip's power supply is brought to 3.6V with a V_{sg} of 1.5V and a V_{tun} of 3.6V while the drain is brought from 3.6 to 0 and 3.6 again with 5 seconds spent at 0V.

Problems arose though, apparently from charge leakage at the floating gate. If a transistor was tunneled to have a to a large offset and low current, it would leak over time to have a larger current, seen in Figure 2.4(a). Oppositely, Figure 2.4(b) shows movement when a transistor was injected to a large current and it started drifting to a lower current level. These effects severely limited the testability of the system which depended heavily on them holding charge.

Figure 2.5 shows the first analog floating gate utilization on the the chip. A follower connected amplifier uses a analog floating gate elements to produce various voltage outputs. Each floating gate in a row is programmed to a different offset and then they are switched in one at a time to recall each needed voltage. Figure 2.6 shows an attempt to program eight elements in a row to a sine wave appearance. Elements during this process unfortunately moved as others were being programmed. Aside from the movement movement, the analog memory block was operational and transitions from one stored coefficient to the next were less then 10us even when measured off-chip.



(a)



(b)

Figure 2.4: Current movements. (a) shows movement of drain current in a floating gate transistor which was tunneled to a low current level. (b) shows the same for a transistor which was injected to produce a high current level.

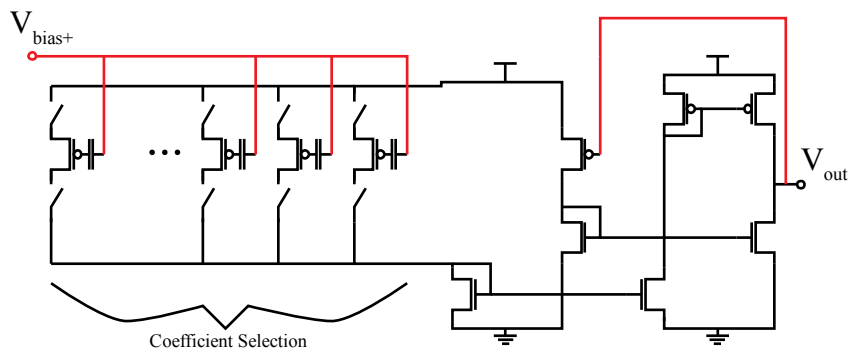


Figure 2.5.: Analog memory system for storing values on floating gates and recalling them as voltages.

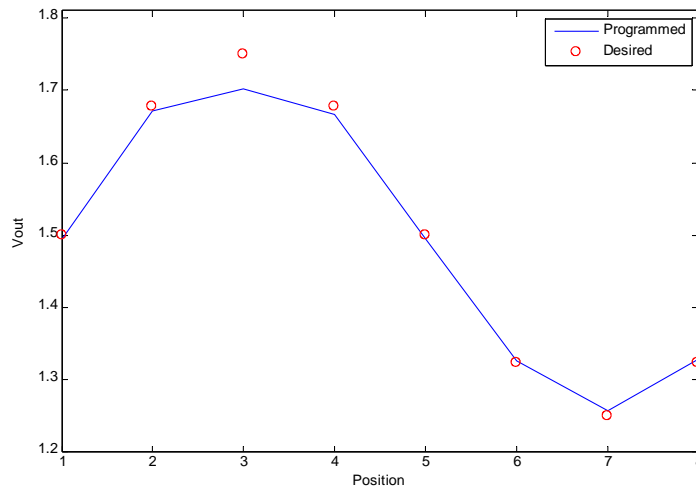


Figure 2.6.: Programmed values in a array of floating gates.

3. Readout Circuitry

The readout circuitry is used to sense the current levels coming from a row of pixels. First, it serves as an active cascode, or rather a low small signal resistance, to fix the voltage of the readout line of a row of pixels. Without this, the small transconductance of the pixels must charge and discharge the large line capacitance. This structure allows the voltage to stay fixed so that all of the current from the pixels comes through the sensing circuitry and is not wasted on the the line capacitance. Secondly, the readout circuitry performs an logarithmic I-V conversion. A logarithmic compression is useful for handling dynamic current ranges of over many orders of magnitude.

The structure for the current sensing readout circuitry and the testing setup for it are shown in Figure 3.1. The two transistors shown are operating in subthreshold saturation which has a relation described roughly by Equation 2. The main point here is that channel current is exponentially related to gate voltage and conversely the gate voltage is logarithmically proportional to channel current. The feedback of the structure fixes the input current line at a voltage V_{ref} . Now, with the source of the sensing transistor fixed, the gate, V_{out} , becomes a logarithmic representation of the input current.

$$I = I_0 e^{\frac{\kappa V_g - V_s}{U_t}} \quad (2)$$

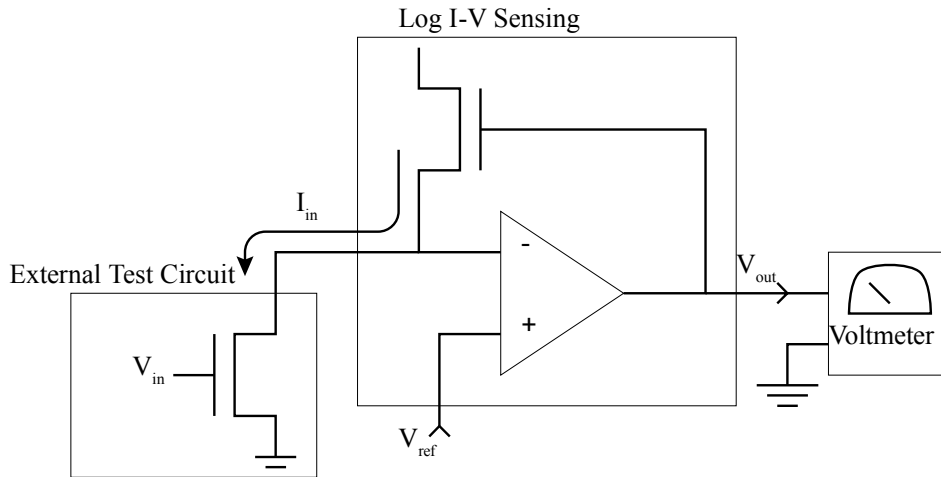


Figure 3.1: Readout circuitry and testing setup. The output V_{out} is logarithmically related to the input current.

In the testing procedure, an external transistor was used to supply a input test current. Operating in subthreshold, the current produced is exponentially related to the applied voltage, V_{in} . Figure 3.2(a) shows the exponential V-I relation in a semi-log plot. The corresponding I-V behavior of the sensing structure produces a linear relation of V_{in} to V_{out} . Though the amplifier worked with a good DC characteristic, it unfortunately suffered from stability issue. Being a feedback system, the open loop poles C/g_m at the input $C_{out} * R_{out}$ and the output caused an instability. In regular system operation, C_{in} is the current output line of the pixel array and C_{out} is a long output line, both of which have several parasitic junctions. $1/g_m$ comes from the sensing transistor and R_{out} is from the amplifier. Unfortunately since g_m changes with current, the system became unstable when smaller currents came from the pixel array. Though steps were taken in design to avoid the instability, which worked in simulation, the system did not perform well in operation. To resolve this, a buffer placed at the output to minimize C_{out} will fix the problem.

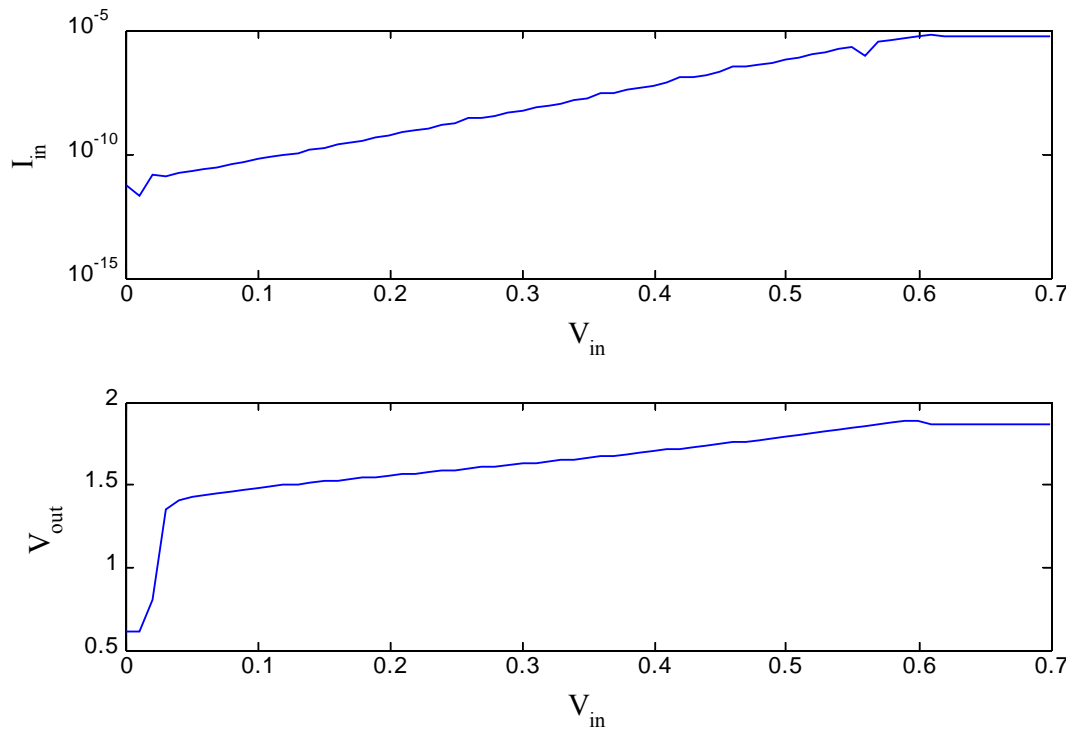


Figure 3.2: Readout circuitry transfer characteristic. The first plot shows the exponential current relation of transistor used in subthreshold operation. With the current from the first plot given to the readout circuitry, the second plot shows that the readout circuitry performed a logarithmic operation to make V_{out} and V_{in} a linear relation over a large range of currents.

4. Pixel Array

The pixel array's operation is centered around a computational sensory element depicted in Figure 4.1. Light is converted to a current through use of a photodiode, which is just a reverse-biased diode exposed to light. This current is used as a tail reference current of a differential pair. The differential output $I^+ - I^-$ is approximately as a hyperbolic tangent:

$$I^+ - I^- = I_{ref} * \tanh\left(\frac{\kappa * (V^+ - V^-)}{2U_t}\right) \quad (3)$$

which becomes a linear function near zero:

$$I^+ - I^- \approx I_{ref} * \frac{\kappa * (V^+ - V^-)}{2U_t} \quad (4)$$

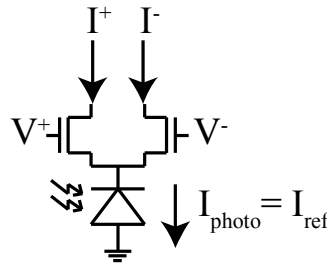


Figure 4.1.: Computational pixel capable of sensing light and performing a multiplication

Using the readout circuitry discussed in Section 3 to measure the current outputs, a sweep of the differential input $V^+ - V^-$ was performed. First V_{out}^+ and V_{out}^- were measured, which are logarithmic representations of the respective output currents. This is seen in Figure 4.2. The result of taking the difference of the exponentials of each voltage produced the expected behavior with a linear region near zero for implementing a multiplication. As seen from the data, the outputs were very noisy. This noise is believed to be a result of the instability of the readout circuitry, discussed already in that section. In fact, this data came from oversampling and averaging and was very slow. The speed of the data and noise level of the collection made large scale pixel plane characterizations too difficult. To verify basic behavior though, a small sample image read is shown in Figure 4.3. The projected image in this case was a circle on a solid background. Here again we see a lot of noise. We were at least able to show functional row and column selection abilities and remove column offsets typical to CMOS imagers. This pixel array utilized added switches in the pixel array to reduce line capacitances, which, again, behaved properly.

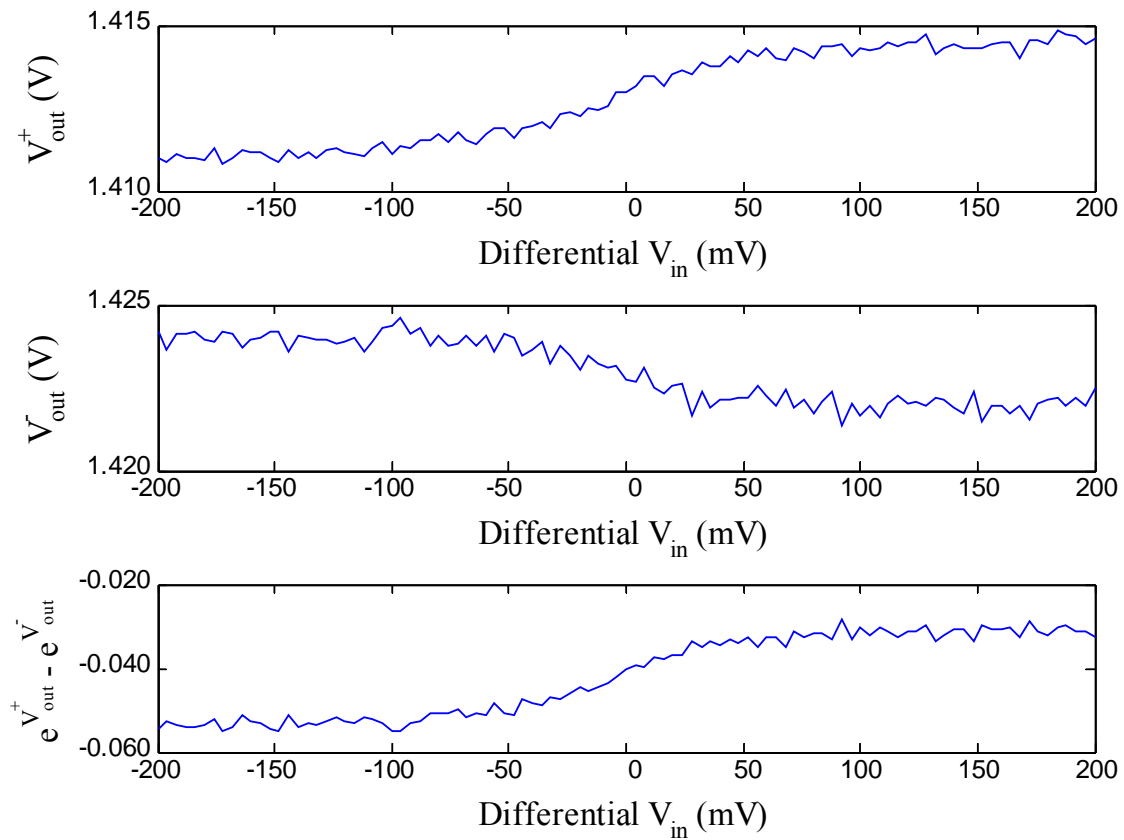


Figure 4.2.: Pixel sweeps. The first two plots show voltage outputs from the logarithmic sensing readout circuitry. The final plot shows the subtraction of the exponentials. The middle region shows the desired linear range which is used for multiplication functionality.

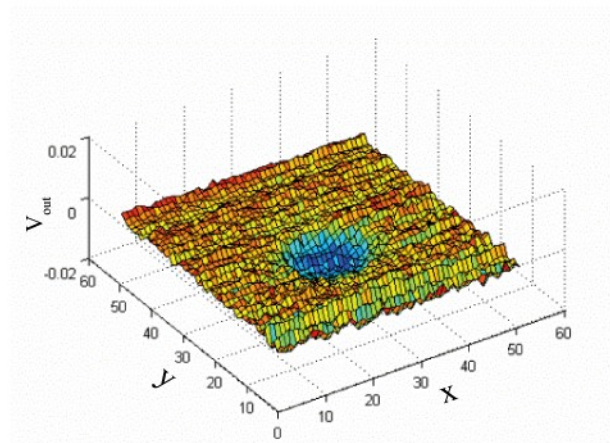


Figure 4.3.: Output from reading array with an image of a circle on a solid background.

5. Conclusion

Discussed here were several results taken from the fabricated chip. Testing ran much longer than expected, in particular to deal with instability in the readout circuitry. Several steps had to be taken to isolate the problem. Sitting at a critical point in the system, it limited ability to get good data from the pixel array or test the following structures which built around the readout sensing behavior. Also, likely contributing to the instability of the system are the lowered current levels from salicided pixels. We believe this lowers the reception of light by the photodiodes and needs to be removed in future fabrications. As discussed, the open-loop poles of the feedback system in the readout move with current level, and get too close when current levels are low.

Among some details not discussed here were some characterizations on the array behavior of the readout circuitry. In particular, small headroom and mismatches made it difficult to bias the 2048 amplifiers with shared bias voltages. Structures will be used in future designs with emphasis on allowing for operation when the structures are mismatched. A final structure on the chip, an integrating current to digital conversion also worked though not carefully detailed here for performance.

Finally, left with apparent movements in floating gate charges, the testing moved to a conclusion. Oxide qualities or perhaps residue from the saliciding process may have caused the leakage. Regardless, we identified key operations in the system though full speed transient behaviors were difficult to obtain. We will have to avoid saliciding for pixels and likely should be also be avoided for floating gates until the effects are detailed more. Functionally, the redesigned pixel array worked and offers a lowered line capacitance for larger imagers. Importantly, we identified several areas for design improvements to increase robustness. With information and insight from this chip, future designs will be greatly improved.