

Characterisation of Advanced Multilayer De-embedding Structures and HBT Devices up to 50 GHz

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Design Number: 72519

Fab-ID: *T52GAH*

I. INTRODUCTION

This report describes the results obtained for measurements carried out on a chip fabricated through Mosis under the MEP research programme (Design Number: 72519, Fab-ID: *T52GAH*). The fabricated test structures are described in section II. Measurement of fabricated passive devices are given in section III, while section IV presents the measurements of active devices. Firstly, however, it is important to put this work in context with previously published material. Coupled with the advancements in the performance of active device technologies of modern semiconductor processes there has been a simultaneous increase in the number of metal layers which allow for more intricate signal routing techniques for RF device characterisation. This work focusses on the development of optimum de-embedding test structures for measurement of a SiGe HBT (emitter area = $1.25\mu m^2$) on IBM's $0.24\mu m$ 6HP BiCMOS technology [1]. This process has 6 metal layers, including a thick top metal layer tailored specifically for high Q applications. The well know four step procedure, requiring a total of 5 de-embedding standards, is employed to de-embed the DUT [2]. Figure 1 shows the structures required to implement the four step de-embedding procedure. Figure 2 shows an impedance based model of the parasitics of structure 1 of figure 1. Structures 2 to 5 are used to characterise and remove each of the parasitics in order to obtain accurate DUT data. The standard approach to de-embedding uses just one metal layer [2] while more sophisticated approaches have proposed ground planes [3] or co-ax type arrangements [4]. While these approaches have been studied up to 30 GHz, here we examine the behaviour of a wide variety of structures up to 50 GHz.

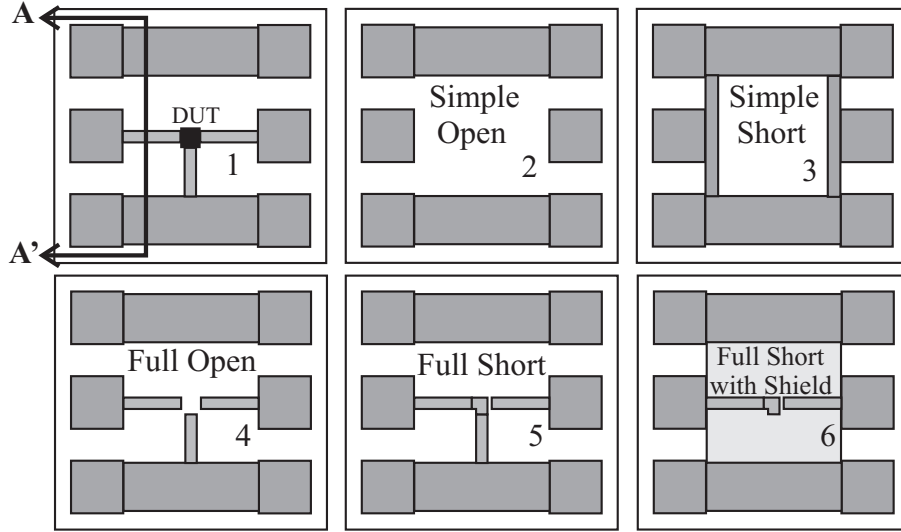


Fig. 1: DUT and corresponding de-embedding structures

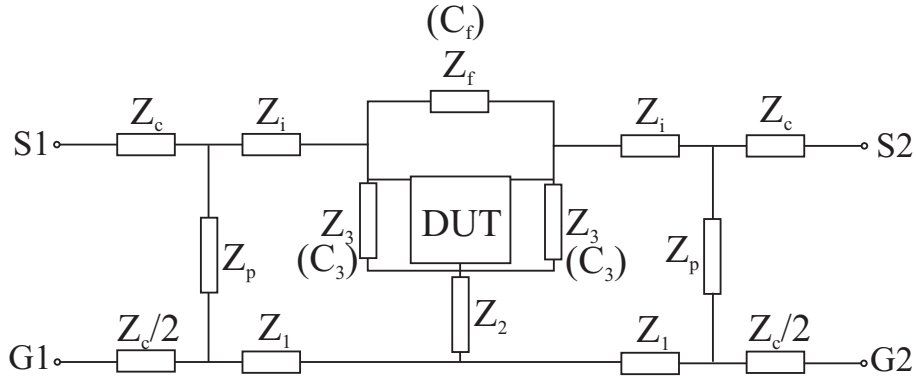


Fig. 2: Representative impedance model of test structure parasitics

II. TEST STRUCTURE OPTIMISATION

In order to take advantage of the 6 metal layers (metal 1 to metal 6) available in the BiCMOS process, five different test structures have been developed. For each HBT and test structure set, another 4 de-embedding standards, specific to each test structure, have been fabricated (total of 25 test structures). Figures 3 and 6 show cross-sections of the region AA' of the DUT structure of figure 1 for each of the fabricated structures.

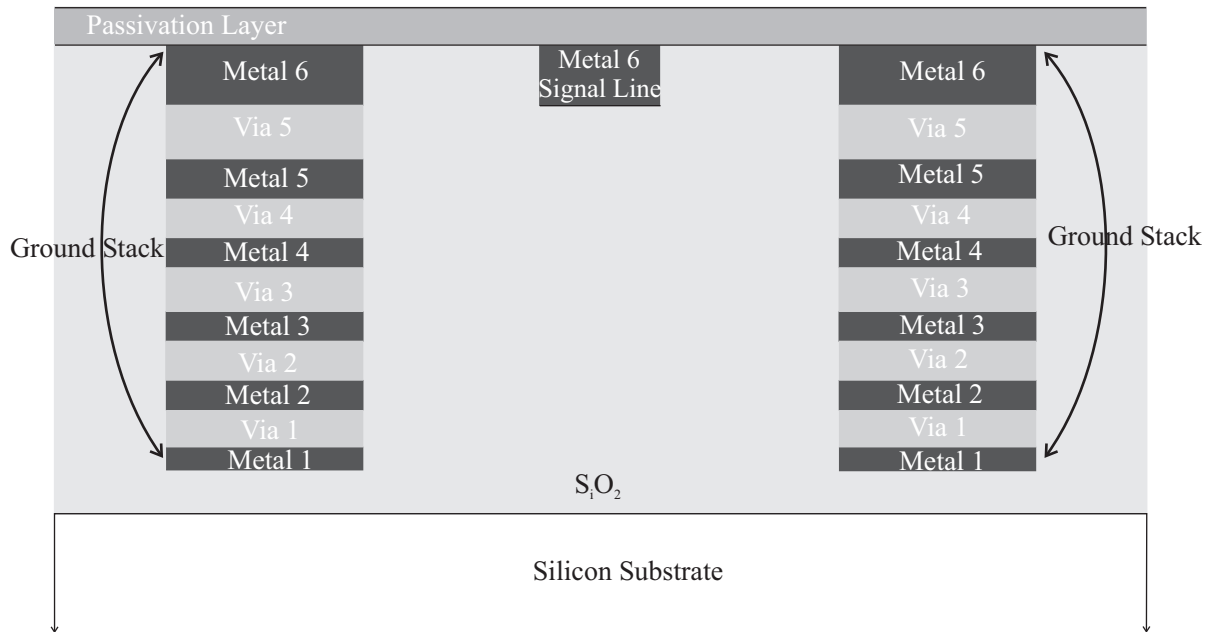


Fig. 3: Standard test structure

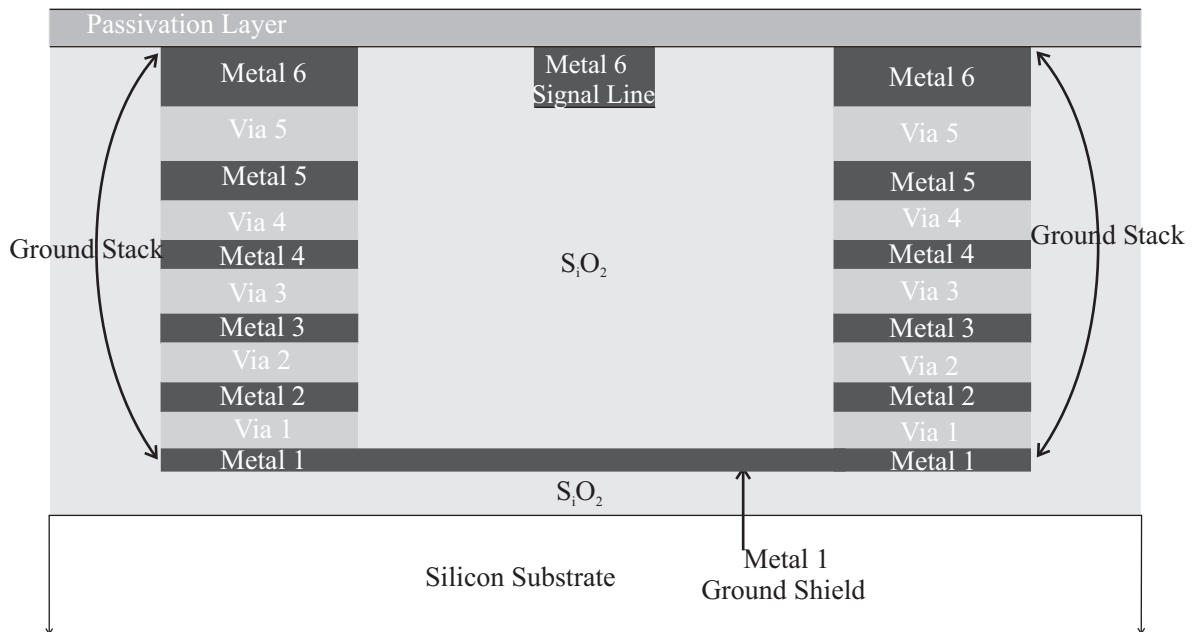


Fig. 4: M1 ground shielded test structure

Figure 3 shows the most basic of the de-embedding test structures that employs just one metal layer for signal routing (standard structure). The shield based structure of figure 4 utilises the lowest layer of the process, metal 1, to provide a substrate shield for the signal line (M1 structure). A similar structure, using metal 5 as the substrate shield, has also been fabricated (M5 structure). More advanced test structure cross-sections are shown in figures 5 and 6. Figure 5 illustrates a structure that utilises the lower five metal layers and corresponding via interconnects to form a stacked ground plane underneath the signal line (stacked structure). A structure, similar to that presented in [4], is shown in figure 6. In this case the signal line, metal 5, is completely surrounded by a ground shield to form a type of on-wafer coaxial environment (surround structure).

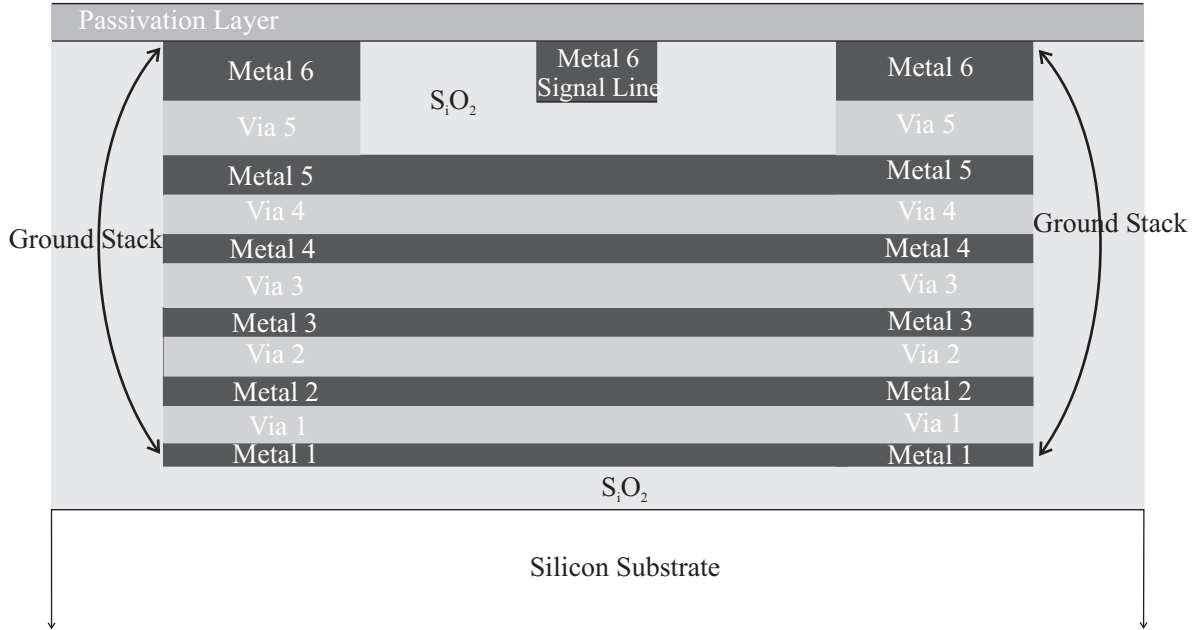


Fig. 5: Stacked structure

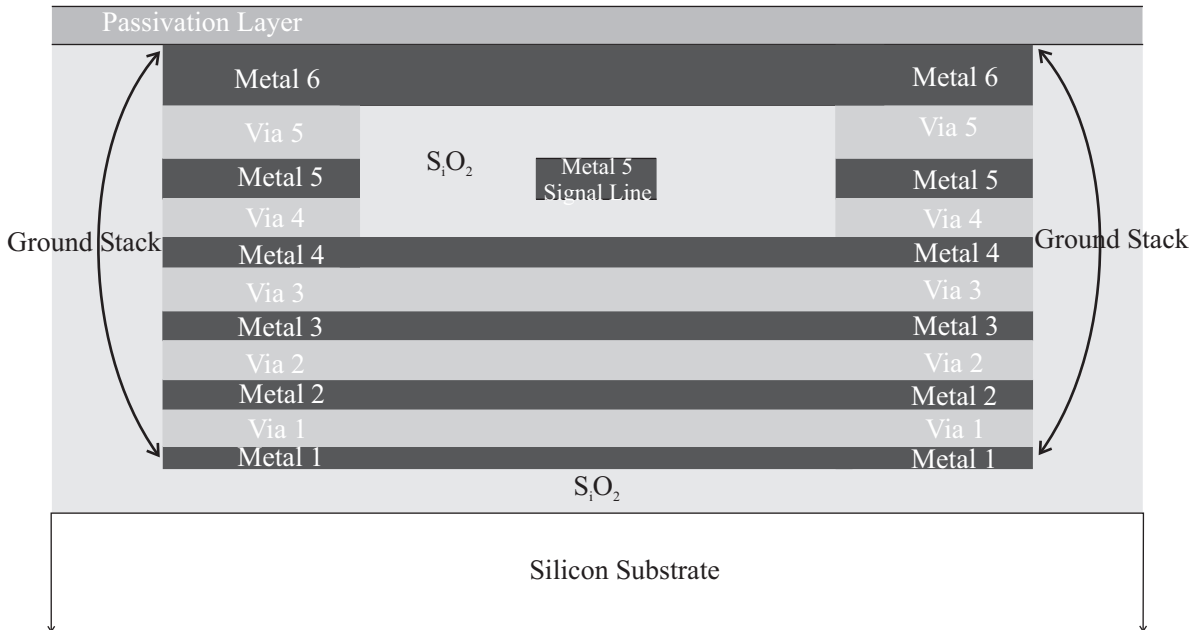


Fig. 6: Surround structure

III. MEASURED TEST STRUCTURE PARAMETERS

Detailed s-parameter measurements have been carried out from 500 MHz to 50 GHz us a HP8510C network analyser. Each of the parasitics of the test fixture model of figure 2 can be extracted and analysed using the de-embedding structures of figure 1. Detailed analysis of the parasitics of the RF signal pads, Z_c and Z_p , has been investigated in many previous publications. This work focuses on the test structure parasitics beyond the pads that are a result of the connection to the intrinsic DUT terminals. The full open and full short de-embedding structures are used for this purpose. The full open standard is used to extract the parasitics labelled Z_f and Z_3 in figure 2. Figure 7 shows the forward coupling, s_{21} , for each of the five different full open standards (Standard, M1, M5, Stacked and Surround) from 500 MHz to 50

GHz[†]. As the HBT device is very small the fixture gap separating the input and output signal lines is only 7.0 μm .

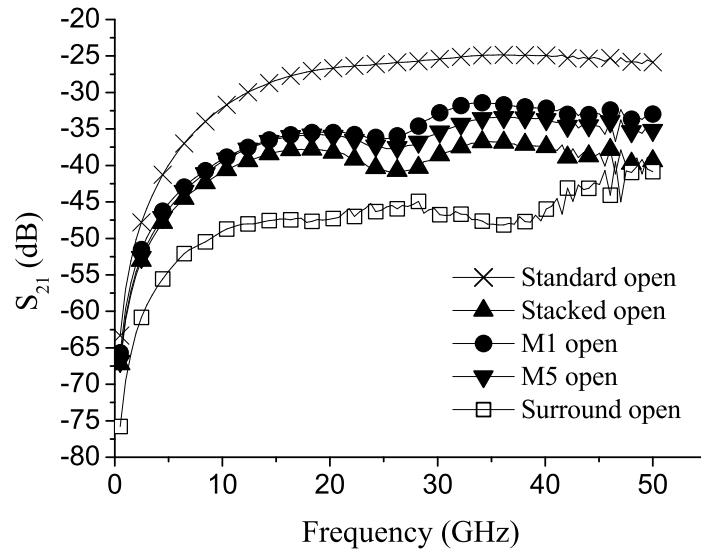


Fig. 7: S-parameter measurement of open standards

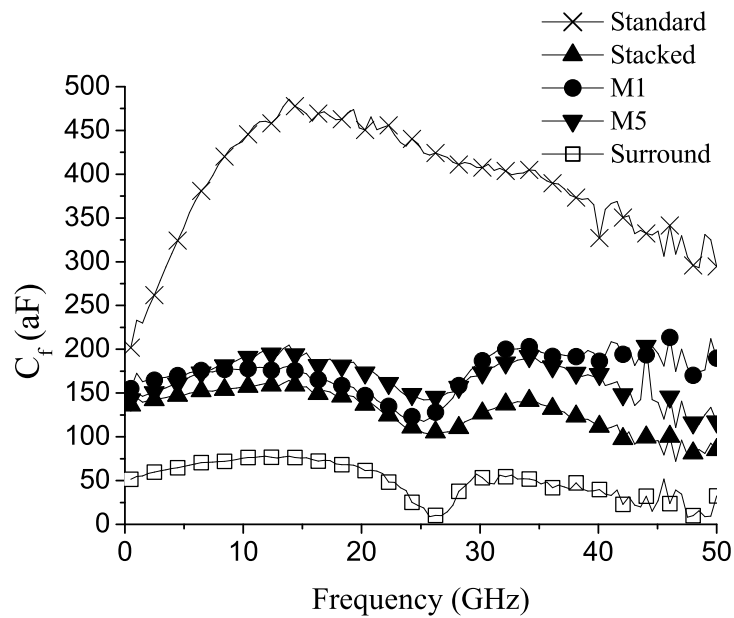


Fig. 8: Extracted forward coupling capacitance

[†]Note that the symbols in the graphs are not shown for every measured data point so that each symbol can be easily discerned

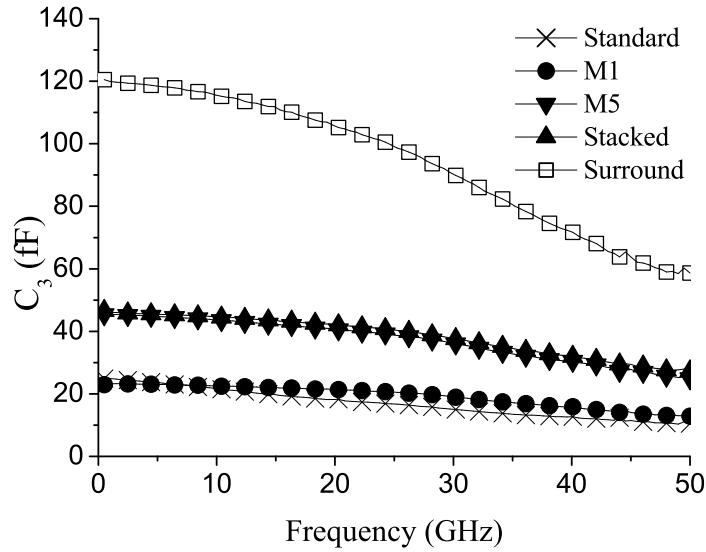
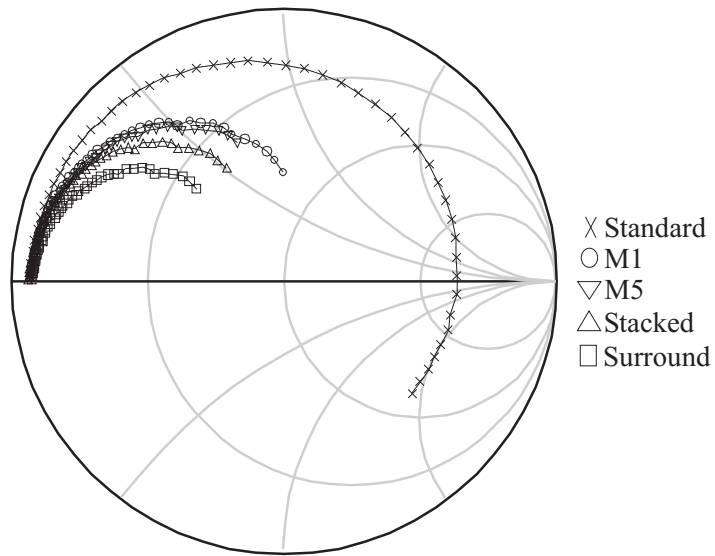


Fig. 9: Extracted ground coupling capacitance

As seen in figure 7 the stacked structure offers improved isolation over the standard, M1 and M5 structures. Even greater isolation between input and output ports is achieved with the surround structure. The effect of this increased isolation can be illustrated more clearly by analysing the forward coupling capacitance of each structure. C_f , the coupling capacitance from the base terminal of the HBT to the collector terminal, is shown for each of the test structures in figure 8. The surround structure achieves the lowest level of forward coupling capacitance and also displays the least variation over frequency. The parasitic, Z_3 , is the coupling capacitance from the input (base) and output (collector) signal lines to the emitter ground line connection. The extracted ground coupling capacitance, C_3 , is illustrated in figure 9. Due to the top and bottom metal ground layers of the surround structure, the surround structure has the largest ground coupling capacitance which is the only apparent disadvantage of this structure.

The impedance model of figure 2 shows that the signal tracks contribute the parasitics labelled Z_i , Z_2 and Z_1 . These parameters are measured using a full short standard (structure 5 of figure 1). Figure 10 shows an s-parameter plot of the input reflection co-efficient, s_{11} , of each of the 5 different test structures. Increases in resistive and inductive components of a line are characterised by an increase in the radius of the Smith chart response. In the standard full short structure (structure 5 of figure 1) a long metal line is needed to connect the intrinsic emitter terminal to the ground pads. For the shield based full short (structure 6 in figure 1) this long length of line is not required as the connection from the emitter terminal to ground can be made directly to the ground shield using a stack of vias. Hence the Smith chart response is much improved once a shield based structure is employed as evidenced by the smaller circles on the Smith chart. Figure 11 shows the extracted resistance for 4 of the short standards[‡]. The surround, stacked and M5 structures provide the least resistance. In terms of inductance, the surround structure out performs all other structures and provides the greatest immunity to frequency variations (figure 12).

[‡]Note that the measured results for the M5 structure have not been included in figure 11 for reasons of clarity as the curve sits very close to that of the surround and stacked structures



freq (500 MHz to 50 GHz)

Fig. 10: S-parameter measurement of short standards

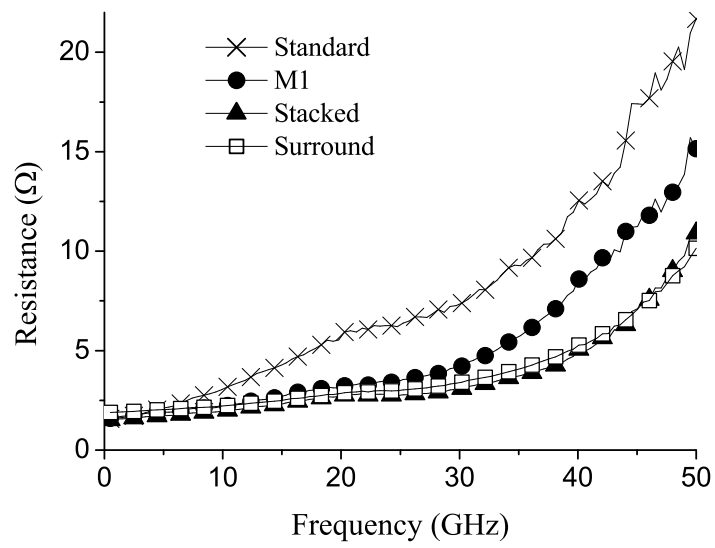


Fig. 11: Short standard extracted resistance

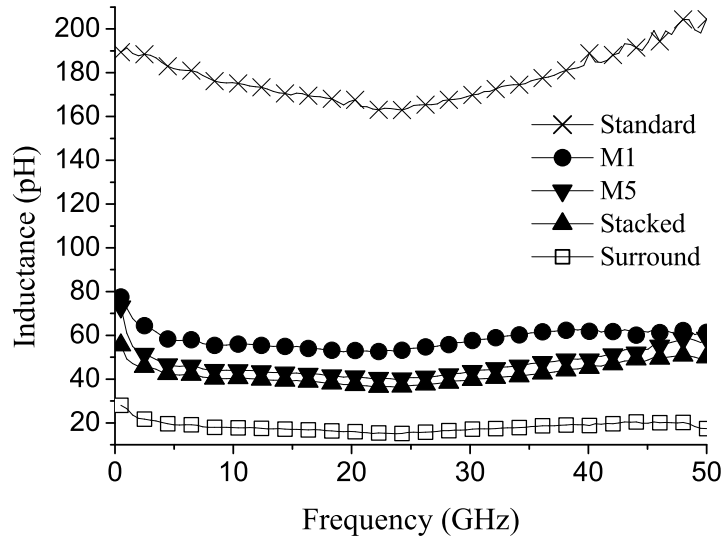


Fig. 12: Short standard extracted inductance

IV. HBT MEASUREMENTS

This section presents measured results for the fabricated HBT transistors. Transistors, embedded within the 5 different test structures were fabricated. In each case the test structure parasitics were de-embedding from the raw measured data. Figures 13 to 17 illustrate the extracted small signal gain, h_{21} , for each of the HBT devices from 500 MHz to 50 GHz. As can be seen very consistent results are achieved. The measured data follows the theoretical -20 dB roll-off very closely in all cases.

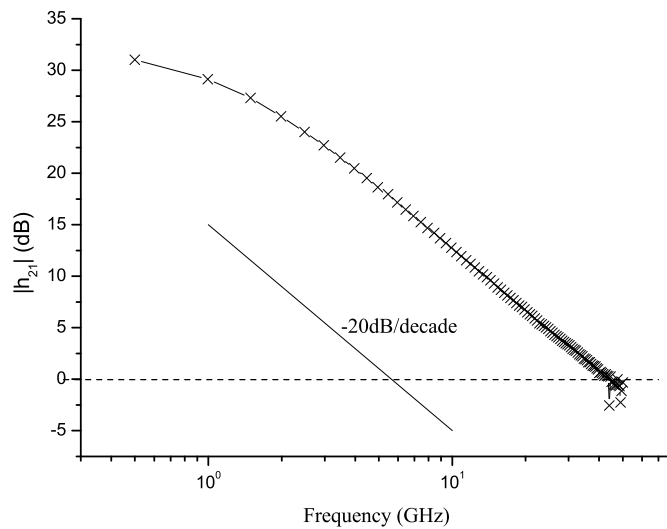


Fig. 13: De-embedding HBT $|h_{21}|$ for standard test structure

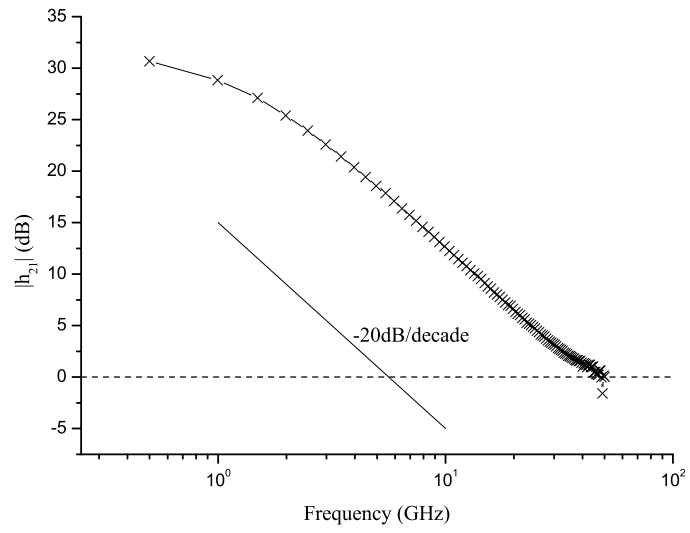


Fig. 14: De-embedding HBT $|h_{21}|$ for M1 test structure

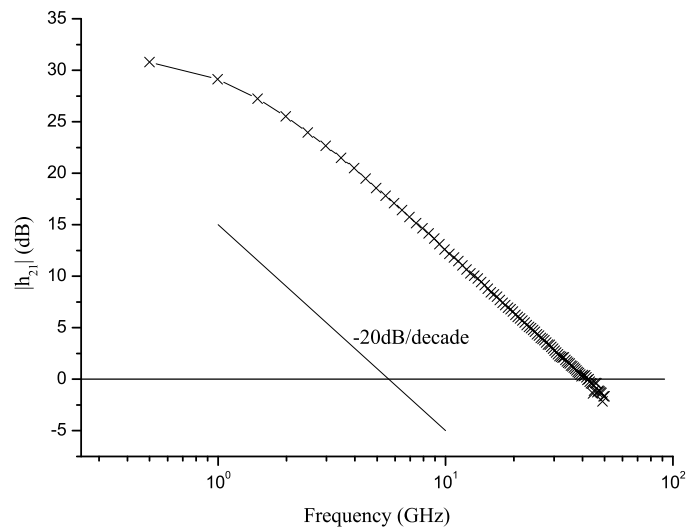


Fig. 15: De-embedding HBT $|h_{21}|$ for M5 test structure

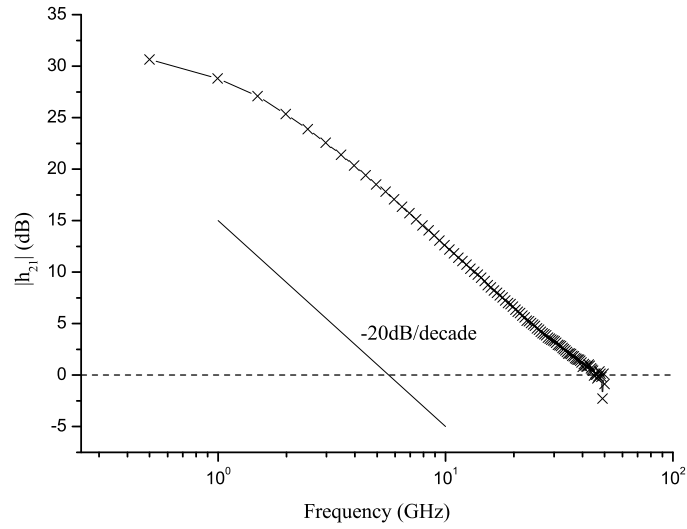


Fig. 16: De-embedding HBT $|h_{21}|$ for stacked test structure

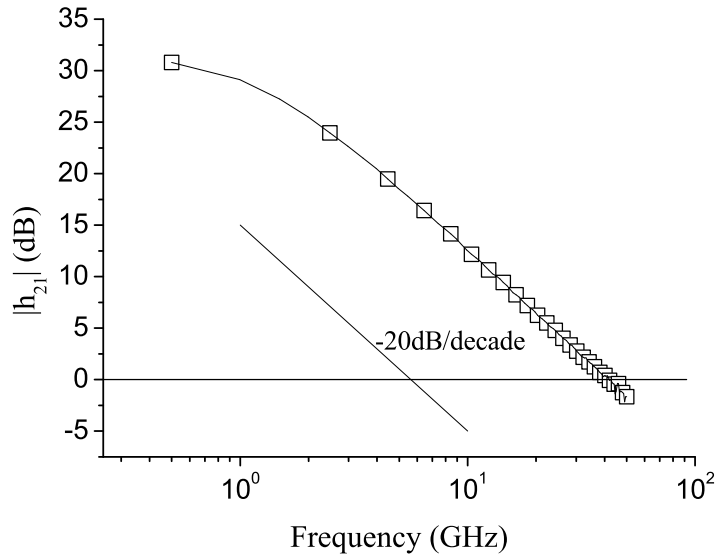


Fig. 17: De-embedding HBT $|h_{21}|$ for surround test structure

V. CONCLUSION

Detailed measurements from 500 MHz to 50 GHz on the IBM chip (Design Number: 72519, Fab-ID: *T52GAH*) have been presented. It has been demonstrated that the quality of de-embedding test structures can be improved dramatically using the stacked and especially the surround structures. The isolation levels achieved with the surround structures provides great scope for fabrication of improved scalable de-embedding structures such as that originally presented in [6]. Even though it has been demonstrated that the traditional standard de-embedding structures still achieve very good results, it is judicious to use the best quality structures.

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