

Design for Mosis Educational Program
(Research)
Investigation of De-Embedding Techniques
and Passive Circuit Design up to 50 GHz

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1 Project Description

Due to advances in integrated circuit technology the operating frequency of many radio frequency circuits and systems is increasing rapidly. The mm-wave frequency range is becoming an ever more attractive option for designers due to the large bandwidth that is available. The availability of high f_T transistors that can operate at mm-wave frequencies within a BiCMOS process means that a single process can meet the twin requirements of very good digital performance coupled with excellent high frequency capability.

In order to successfully design mm-wave circuits it is necessary to have highly accurate active device models. Device models are obtained by measuring the device under test (DUT) to obtain the necessary information to construct reliable models. As can be seen from figure 1 a single DUT can be measured by mounting it on a board or by wafer probing it. For device model applications at microwave frequencies measurements are usually performed with the latter technique. On-wafer measurements are typically calibrated using a ceramic impedance standard substrate (ISS) that offers high accuracy and low loss standards for two port calibration procedures such as SOLT, LRRM and TRL [1]. ISS calibration is sufficient in cases where substrate and interconnect losses of the chip containing the DUT are comparable to those of the ISS. This, however, is not the case for CMOS and BiCMOS processes operating at high frequencies. For example, the wafer-probe based test structure shown in figure 1 has a large number of parasitics that are not removed by the ISS calibration. Figure 2 shows a DUT surrounded by a number of impedance blocks that represent the various parasitics associated with a microwave measurement system. The rf pads themselves and the connections to the DUT coupled with the lossy silicon substrate are responsible for all of the induced parasitics. All of these unwanted elements need to be characterized and removed before accurate device model extraction can be undertaken. The first part of this project will involve the design and fabrication of different de-embedding structures. Current state of the art de-embedding methods, [1] [2], demonstrate how accurate de-embedding can be performed up to 15 GHz. This project will expand upon this work by increasing the frequency of analysis to 50 GHz. New and more area conscious structures will also be implemented. A special substrate shielding technique, [3], that has a strong influence on de-embedding circuits and on many other passive architectures, will also be fabricated.

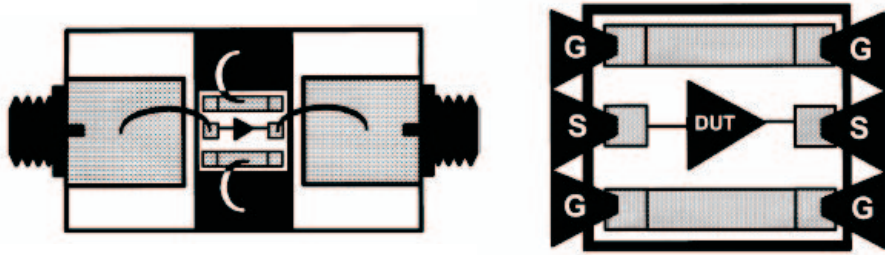


Figure 1: Test fixture options for microwave measurements [4].

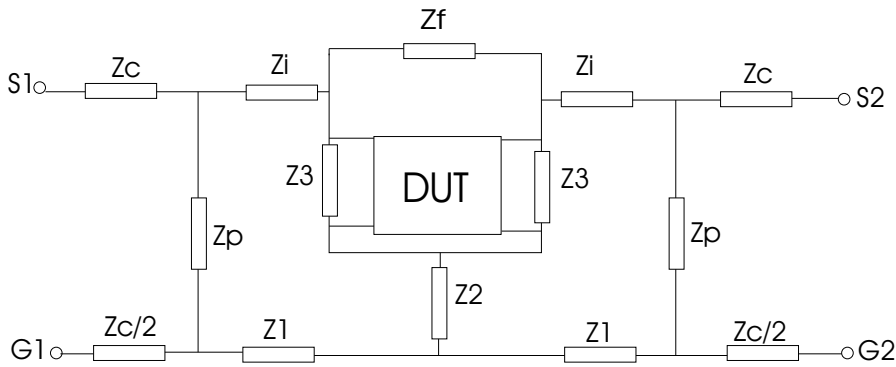


Figure 2: Parasitics associated with the measurement system.

Of no less importance than the need for reliable active device models is the requirement for accurate passive models. Design of high quality baluns is critical for the implementation of such front end components as double balanced mixers [5] and differential low noise amplifiers. Although baluns are a mature and well researched topic from a general view point, [6] [7], very little work has been done on baluns that are built on lossy silicon substrates. Therefore, the second part of this project will focus on the design of mm-wave baluns suitable for applications between 30 GHz and 40 GHz. Being able to design with a process that offers many metal layers is a very attractive proposition for the design of baluns. The basic building blocks of mm-wave microstrip baluns are couplers. Using a process with a number of metal layers gives the designer a lot of scope to achieve very tight coupling and hence good balun performance. Therefore, a number of different balun architectures will be investigated and fabricated. Some of the couplers used to make up these devices will also be fabricated to aid in the successful analysis of the baluns during the test process. A balun is a differential to single

ended device and, hence, the de-embedding techniques required are different to those of a single ended device. Therefore, as well as fabricating the balun structures a number of other more advanced de-embedding structures will be fabricated. It is intended that these structures will be suitable for the de-embedding of differential to single ended circuits as well as standard differential applications.

2 Fabrication Process

The fabrication process requested is the TSMC 0.18 μm process with the intention of taping out on the run scheduled for 15 November 2004.

3 Packaging Process

These designs will not require any packaging as all of the measurements will be carried out at wafer level.

4 Estimated Project Size

For the first part of this project a number of de-embedding structures will be required. In order to fully implement the most advanced methods, [1], and to incorporate a number of new and more novel shielding structures, [8], a total of 15 structures will be required. Although the active devices that are used to verify the de-embedding method are small, the size of the test fixture is dominated by the rf pads. Given the fact that the pitch of the ground signal ground (GSG) probes that will be used for testing is 150 μm the approximate size of each fixture will be 560 μm by 470 μm . The second part of the project involves differential de-embedding and balun design. Microstrip baluns are designed so that the length of the lines corresponds to $\lambda/4$. For operation at 30 GHz the approximate size of a balun including pads is 1700 μm by 800 μm . It is intended that three different types of baluns will be fabricated. Each differential de-embedding standard will occupy approximately 790 μm by 560 μm . A sample chip layout has already been done with Cadence's Virtuoso layout editor and it has been found that a chip with dimensions of 5 mm by 5 mm will be required for this project.

5 Simulation Plans

Currently the need to fabricate a number of de-embedding structures along with the actual device under test consumes a large amount of die area. This project will investigate the possibility of implementing the de-embedding analytically by using EM simulators (ADS Momentum and Ansoft HFSS). The first step in this process would be to match the measurement results of the de-embedding test structures with simulations performed on the same structures. This would then mean that the parasitics associated with any measurement setup could be characterized via simulation. The consequences of this type of scenario are very attractive because it would mean that in future there would only be a need to fabricate the actual device under test and valuable die area could be saved by not fabricating de-embedding structures. The design of the balun topologies will be done entirely using EM simulations. Again, once fabrication is complete, direct comparison between the measured and simulated results can be made.

6 Test and Characterization Plans

Wafer probe measurements will be performed up to 50 GHz. Both s-parameter and noise measurements will be performed. The test setup to be utilised is shown in figure 3. All tests will be controlled via a PC and HPVVEE software. This will enable many measurements to be performed quickly and repeatedly. The main elements of the test setup are the *HP8510* Network analyser, with measurement capability to 50 GHz, and a Cascade Microtech probe station. Infinity probes will be used to perform the measurements. Although the network analyser can only be used to measure s parameters, all the other small signal parameters (ABCD,h,y,z) can be extracted from the initial s parameter measurement. The noise performance of the active devices will also be carefully analysed up to 50 GHz using a noise figure meter (*HP8970A*), noise source (Agilent 346C) and an external mixer.

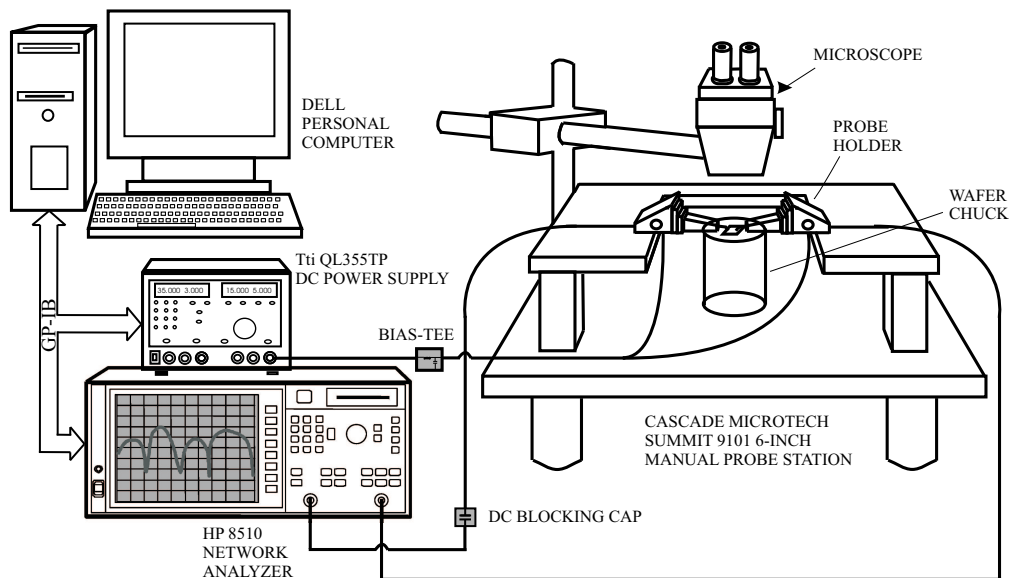


Figure 3: Laboratory Test Setup

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