

A Low-Power Cochlear Implant DSP Microsystem with Hybrid LC Clocking

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Increased integration of components into a single SoC will enable performance improvements in bio-medical applications. The microsystem described here combines an energy-efficient MCU, the first reported cochlear implant (CI) algorithm-specific DSP core and a self-referenced hybrid *LC* oscillator clock reference into a monolithic SoC intended for use in CIs. By merging all of these components on a single substrate, area and power consumption of the system are greatly reduced compared to present CI systems without sacrificing performance. This makes fully implantable CIs feasible in the near future; something that is not possible with traditional CI approaches due to size and power requirements. This SoC has been developed as part of the Wireless Integrated MicroSystems (WIMS) Engineering Research Center (ERC).

This work constitutes a significant expansion of a previously reported microsystem [1]. Extensive modifications to the MCU architecture and instruction set have been implemented; the CI DSP core is a major addition to the previous SoC and significant performance improvements to the clocking scheme have been achieved. Fig. 1 shows the microsystem architecture consisting of the digital MCU, DSP core and the all-silicon clock synthesizer as part of the proposed fully implantable WIMS CI. The MCU includes a 3-stage pipeline, 16-bit datapath, 24-bit unified instruction and data address space,

32kB of on-chip SRAM, a 512-byte loop cache and an external memory port supporting up to 128kB. Communication between the DSP and the MCU consists of shared memory space for coefficients, control registers and shared serial peripheral interfaces for communication with the implant electrodes and the external ADC. A software-controlled memory-mapped register selects the frequency that the hybrid clock reference supplies to the microsystem.

Within the custom WIMS instruction set, 11 instructions were eliminated and 19 instructions were added, bringing the total instruction count to 85. A majority of the instructions were re-encoded to reduce decode complexity. The new instructions enable the power-aware WIMS compiler to more efficiently manipulate address registers and further expand support for multi-word signed arithmetic. Address and data registers now have separate register window control bits to provide the compiler maximum flexibility when changing windows. The windowing scheme reduces the register-encoding field to enable 16-bit instructions while providing adequate temporary storage [2].

Certain parameters in a CI must be variable to help patients achieve optimal speech comprehension [3]. The most important of these are the filter cutoff frequencies, compression function, number of channels, channel to electrode assignment, pulse duration and pulse rate. Our CI microsystem allows individual patients to be custom fitted by programming each of these parameters via the MCU.

The signed-magnitude fixed-point DSP core has four operating modes. The DSP typically runs in stimulation mode, processing sound samples to generate stimulation pulses. Filter

coefficients, look-up table (LUT) data and the stimulation profile must be set up in programming mode. Test mode provides observability and controllability over each component in the DSP by bypassing datapath stages via multiplexors at the output of each stage. Sleep mode shuts down DSP components to conserve power. While in stimulation mode, the control unit uses the sleep mode circuitry to shut down any unused components. Assuming a 22kHz front-end ADC, which is standard for speech processing within the human audible range of 0 to 10kHz, the DSP must operate at 3MHz to provide adequate data rates for high pulse rate stimulation.

The self-referenced hybrid clock synthesizer, shown in Fig. 2, includes a free-running RF *LC* oscillator, a low power ring oscillator, a temperature-compensated bias circuit and an arbiter [4] for asynchronous glitch-free switching between the two oscillators. The synthesizer supports a reduced-power standby mode in which the *LC* oscillator is powered down while the system operates from the low power, low frequency ring oscillator. The entire clock synthesizer occupies 0.25mm^2 of silicon area.

The RF *LC* oscillator includes a cross-coupled negative-transconductance sustaining amplifier, a differential inductor and a bank of switched capacitors in parallel with the *LC* tank. The *LC* oscillator generates a 1GHz reference signal that is followed by a frequency divide-by-5 circuit. This divisive approach to clock synthesis reduces the relative jitter [5]. Frequency deviation due to process variation can be corrected by trimming the capacitance in the *LC* tank using an 8-bit calibration byte. The measured calibration range is $\pm 10.75\%$, giving an initial calibrated accuracy of $\pm 420\text{ppm}$ at 25°C . The ring oscillator

contains five differential stages and nominally outputs a 20MHz signal that can be calibrated via the digital interface to account for process variation.

An HDL-synthesizeable dynamic clock frequency controller allows the MCU software to adjust the clock frequency to match workload requirements. This circuit, shown in Fig. 3, was coded entirely in Verilog HDL, yet supports low-latency glitch-free clock frequency selection ranging from 78kHz up to 100MHz when used in conjunction with the hybrid clock synthesizer. This implementation provides independent dynamic frequency scaling for the MCU and the DSP cores. Software can select the optimal clock frequency for each component depending on operating conditions by setting the multiplexor control bits. Fig. 4 shows oscilloscope traces of this frequency scaling. The maximum latency to scale operating frequencies with this circuit is 51ns if the ring oscillator is selected, or 6ns if the *LC* oscillator is selected.

The design was fabricated in TSMC's 0.18 μ m mixed-mode CMOS process and contains 2.3 million transistors on a 9.18mm² die. Fig. 5 is a table of the measured performance of the fully functional fabricated microsystem. The microsystem consumes only 1.79mW when operating in CI mode. Fig. 6 shows the wide range of operating points for both the MCU and DSP. Fig. 7 is a die-micrograph of the completed microsystem.

Acknowledgements:

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References:

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- [5] M. McCorquodale, M. Ding and R. Brown, "Top-Down and Bottom-Up Approaches to Stable Clock Synthesis," *Proc. of ICECS*, vol. 2, pp. 575-578, Dec. 2003.

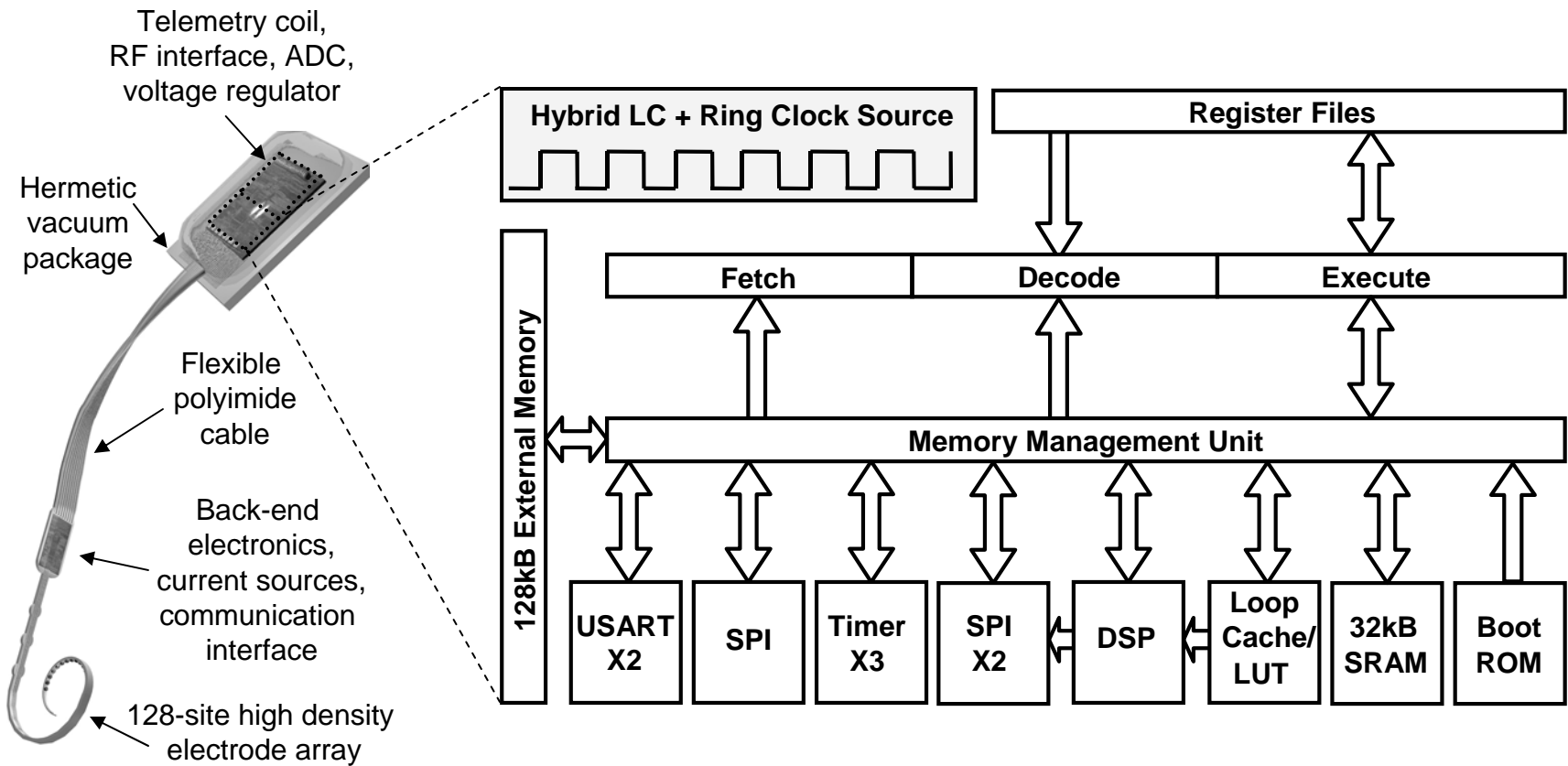


Figure 1: Microsystem architecture as part of the proposed fully implantable WIMS cochlear implant.

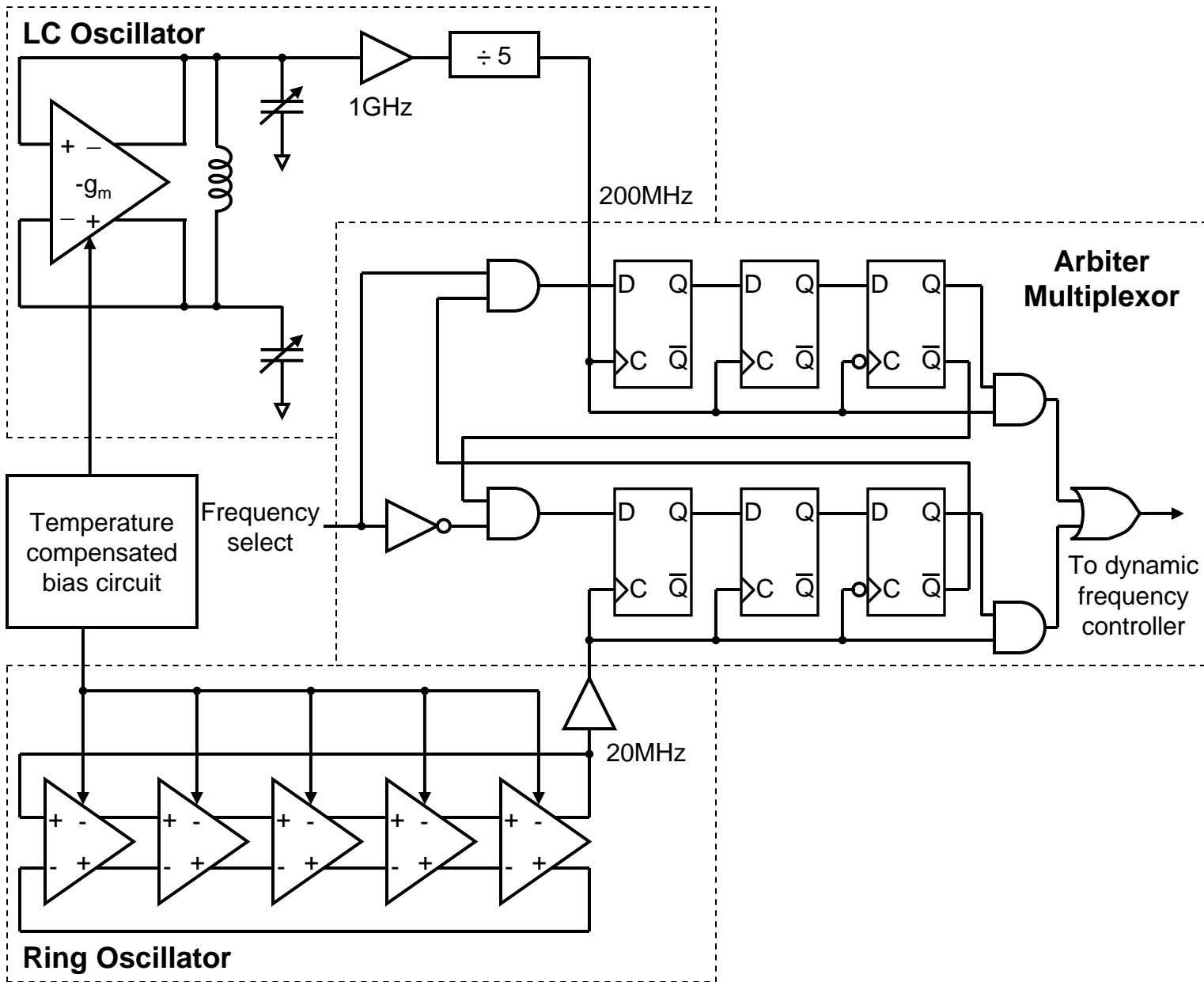


Figure 2: Hybrid clock synthesizer.

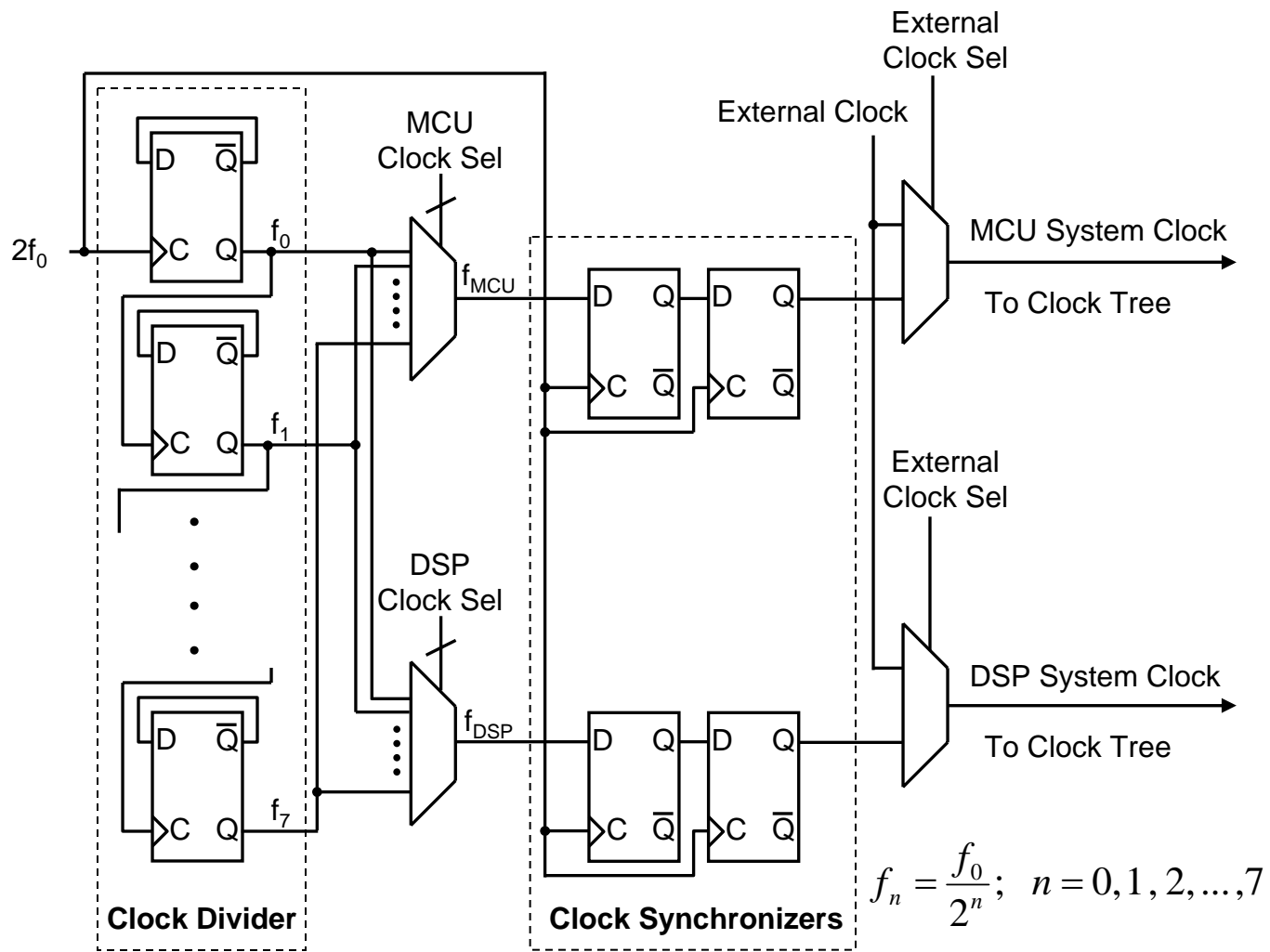


Figure 3: HDL-synthesizable glitch-free dynamic frequency controller.

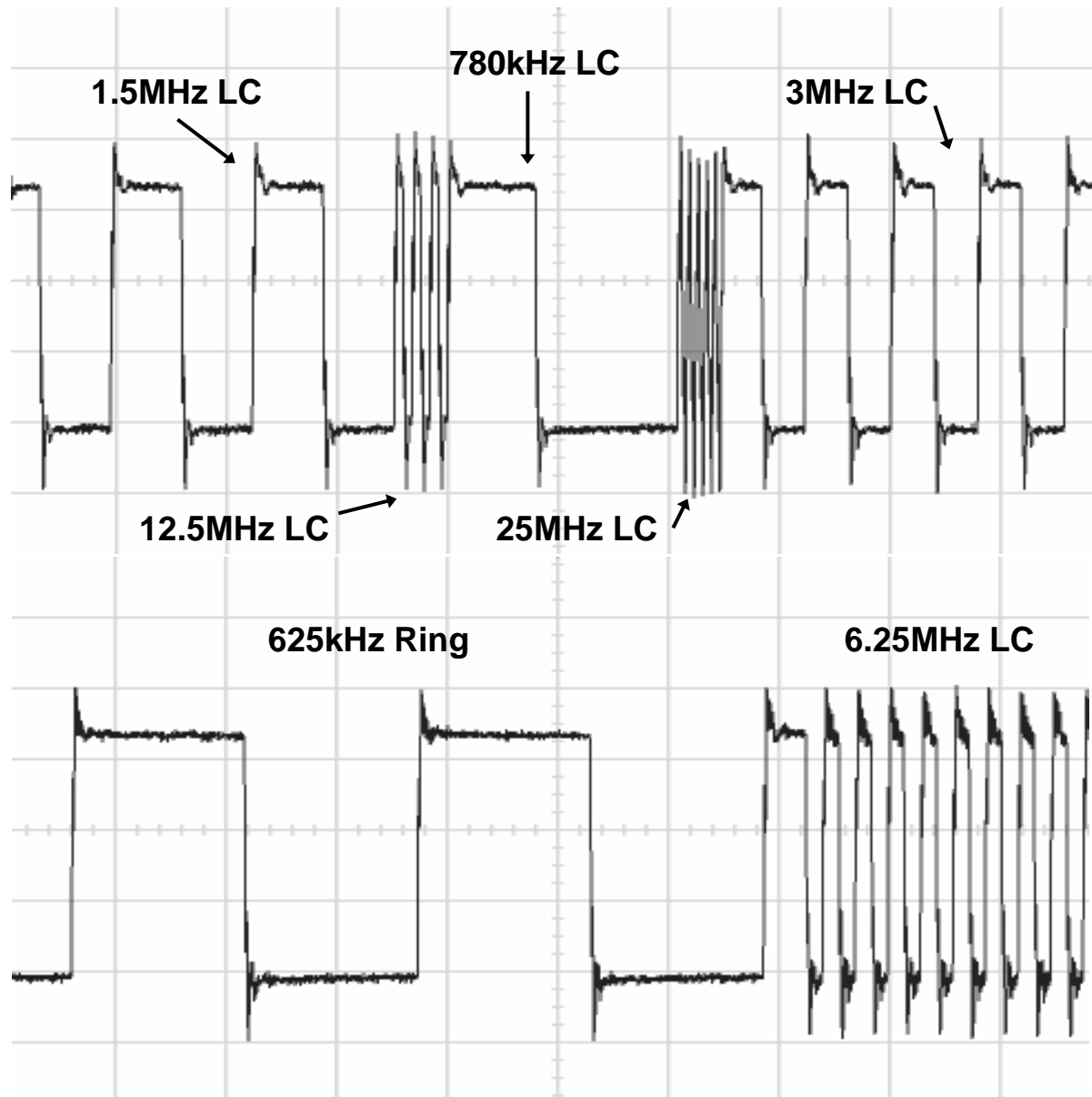


Figure 4: Low-latency dynamic clock scaling oscilloscope traces.

Operating Condition Component	$V_{DD} = 1.8V$			$V_{DD} = 1.2V$		
	100MHz	DSP Mode ^a	Standby	1MHz	DSP Mode ^a	Standby
Core (mW)	25.73	1.63	0.54	0.31	0.44	0.10
Memory (mW)	7.83	0.12	0.12	0.04	0.03	0.03
DSP (mW)	2.46 ^a	2.46	0.27	1.14 ^a	1.14	0.06
Clock (mW)	9.62 ^b	0.76 ^c	0.76 ^c	0.18 ^c	0.18 ^c	0.18 ^c
Total (mW)	45.64	4.97	1.69	1.67	1.79	0.37

- a. DSP is operating at 3MHz. Other components operating at speed necessary to support DSP function.
- b. LC oscillator is operating, ring oscillator is off.
- c. Ring oscillator is operating, LC oscillator is off.

Figure 5: Microsystem measured performance at several operating conditions.

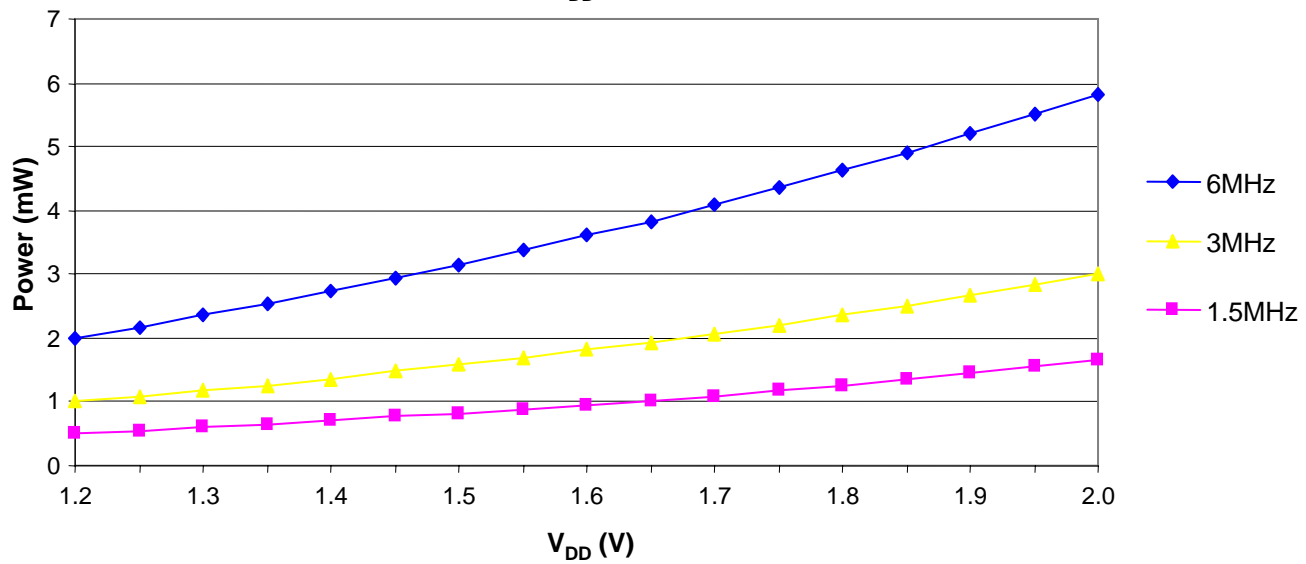
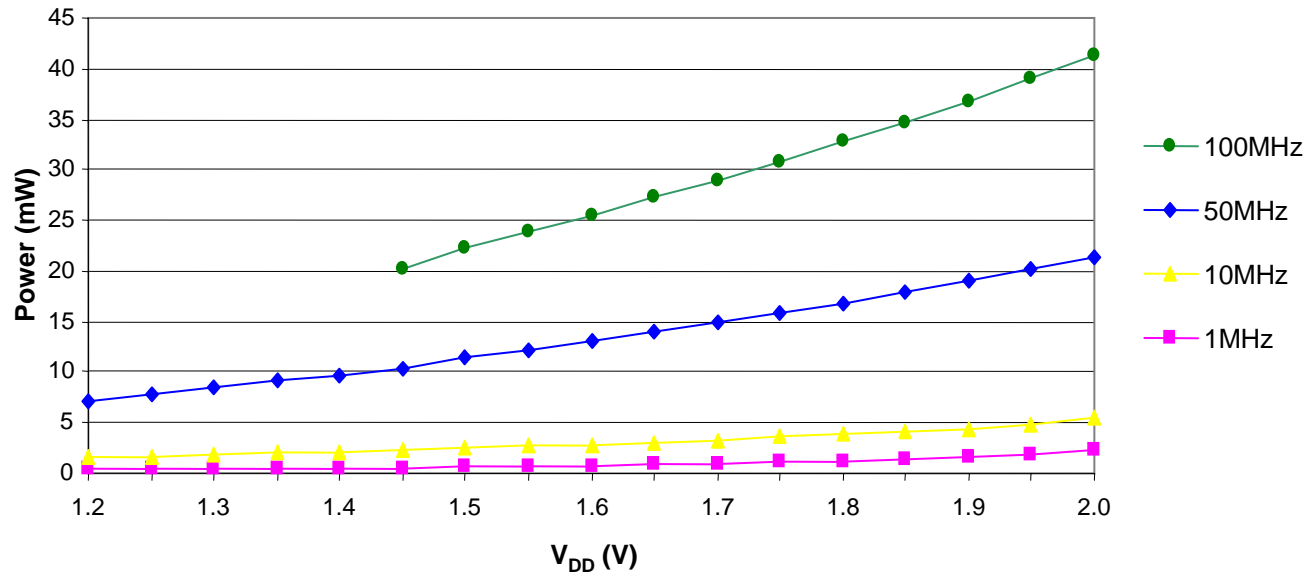


Figure 6: Power versus V_{DD} scaling across different frequencies for the MCU plus memory (top) and DSP (bottom).

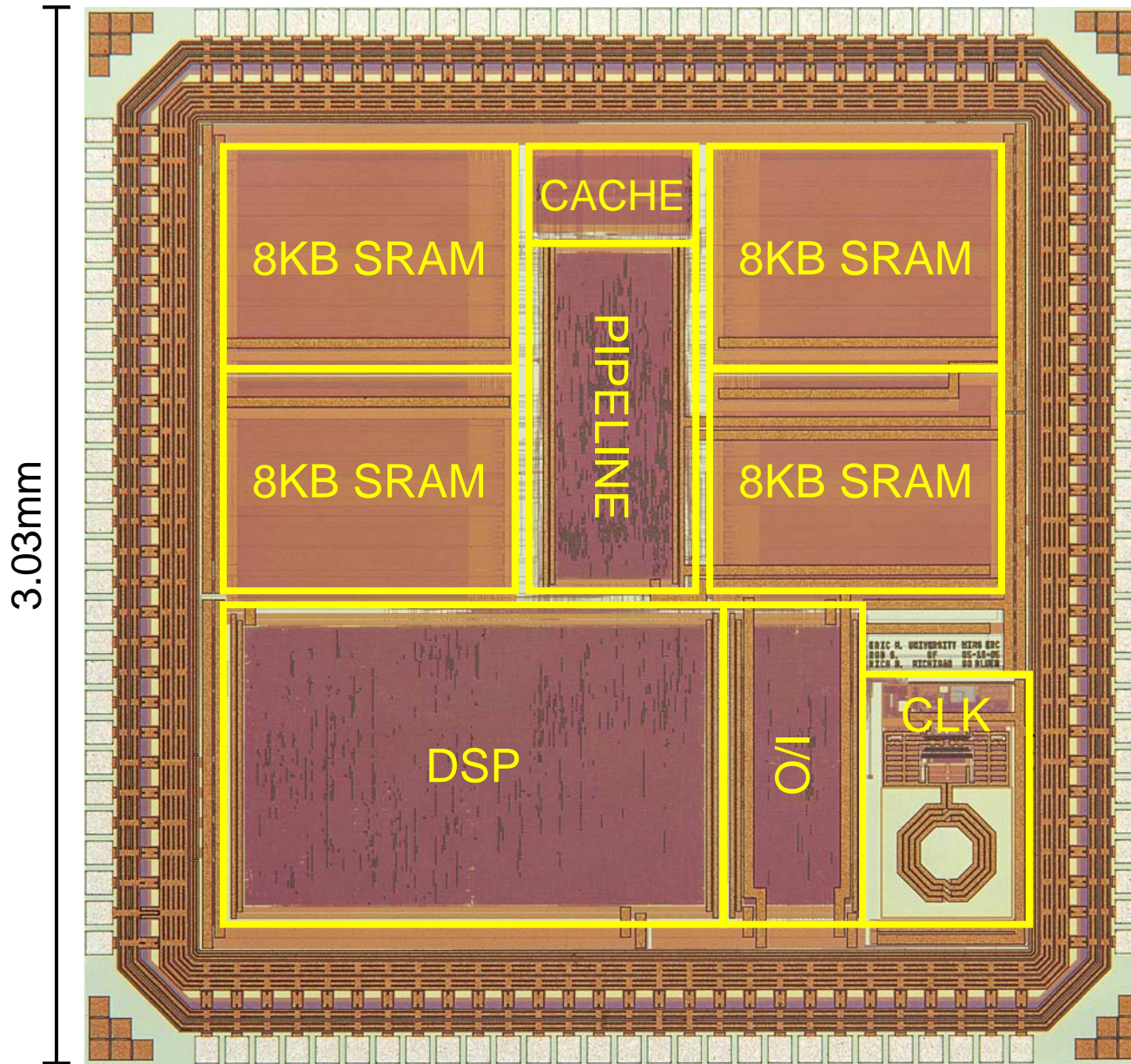


Figure 7: Die micrograph of microsystem in TSMC 0.18 μ m mixed-mode process.