

Design for MOSIS Educational Program (Research)

Design of OTA-Based Window Comparator

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As shown in Figure 1, the proposed design is comprised of a differential input pair and four current mirrors. Transistors N_1 and N_2 constitute the differential pair and their tail current is provided by transistor N_3 . PMOS devices $P_1 \sim P_6$, which have the same size, implement two sets of PMOS current mirrors; while, transistors N_4 and N_7 , N_5 and N_6 , realize two NMOS current mirrors. The size of transistors N_6 and N_7 is m times larger than that of N_4 and N_5 . Assume the tail current flowing through N_3 is I_b . When both comparator inputs are at the same level, transistors N_1 , N_2 , N_4 , N_5 , and $P_1 \sim P_6$ are in their saturation regions, and all the currents flowing through these transistors are $\frac{I_b}{2}$. Devices N_6 and N_7 , working in their linear regions, pull voltages at nodes A and B close to ground, driving the comparator output to logic **1**. When there is a difference between the comparator inputs, currents flowing through devices N_1 and N_2 become $\frac{I_b}{2} + i$ and $\frac{I_b}{2} - i$, or *vice versa*.

Assuming that the relation between I_{DS} and V_{GS} of N_1 and N_2 follows perfect square law, the comparator threshold can be derived as:

$$V_\epsilon = \sqrt{\frac{I_b}{\mu_n \cdot C_{ox} \cdot (W/L)_{1,2}}} \cdot \sqrt{1 - \sqrt{1 - \left(\frac{m-1}{m+1}\right)^2}} \quad (1)$$

where μ_n is carrier mobility; C_{ox} is gate unit capacitance; and $(W/L)_{1,2}$ is the device size of N_1 and N_2 . The above equation shows that the comparator threshold can be adjusted by changing its biasing current. According to this observation, we will also develop different biasing circuits for dynamically adjusting the comparator threshold. So the final design will consist of several comparators with different biasing circuits. Their performance will be evaluated by testing the fabricated chips.

2 Estimated Size

We propose to design and fabricate the proposed circuit using IBM7RF 0.18 CMOS technology. The required fabrication date is June 19, 2006. The estimated area of the chip is $2mm \times 2mm$, and the required package is DIP-28.

3 Simulation Plan

Various simulations will be performed in the project to make sure the layouted circuits function properly. During the schematic design phase, extensive simulation will be carried to optimize transistor sizes. After the layout is complete, post-layout simulations will be performed to verify the circuit function. In both phases, simulation methods will include DC and transient analysis. DC analysis is used to find out the comparator threshold; while, transient analysis is for studying circuit dynamic behaviors, such as delay and the maximum

operating speed. Also, corner and Monte Carlo simulation will be performed to investigate how process variations affect the design.

4 Testing and Characterization

Both the static and dynamic characteristics will be tested after receiving the fabricated chips. To perform static characterization, one input of the comparator under test is tied at various DC voltage levels. The other comparator input is fed with a ramp signal, and the comparator output is monitored by an oscilloscope to find the comparator threshold. The measured values will be compared with design goals. To study comparator dynamic behaviors, both comparator inputs are fed with sine wave signals. Different combinations of the frequency, magnitude, phase of the two input signals will be used in the testing process.