

**Design for MOSIS Educational Program (Research)**  
**An integrated circuit for the realization of a Piecewise Linear Calculation Structure**

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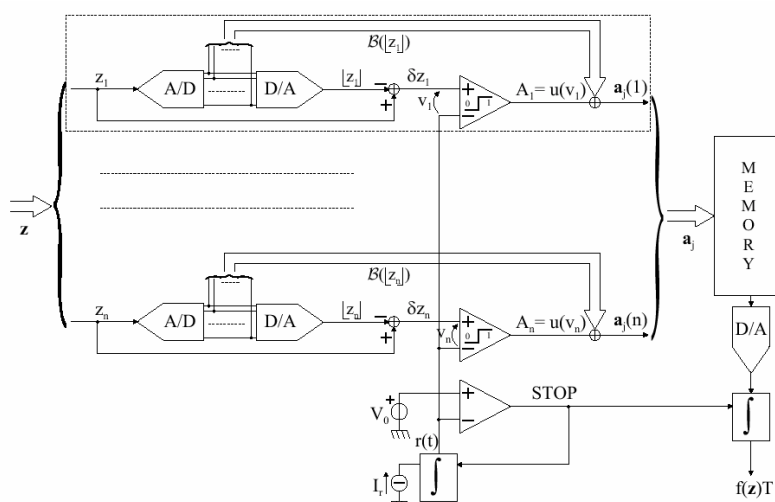
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## Proposal for MEP Research Program:

### An integrated circuit for the realization of a Piecewise Linear Calculation Structure

#### *Project description.*

The objective of this proposal is to fabricate an integrated circuit that implements a three-input Piecewise Linear (PWL) Programmable Calculation Structure like the one described originally in [1]. The circuit provides a programmable platform for synthesizing an arbitrary function of three inputs according to the principles exposed in [2]. This structure constitutes a generic hardware platform for nonlinear function representations, and it can be used together with dynamic and spatial filters to produce nonlinear filters, like the ones proposed in [3] or imagers with built-in processing capabilities like those proposed in [4]. Both structures described in [3]-[4] use as their main cores, a PWL structure like the one described here.



**Fig. 1: Architecture of the PWL Calculation Structure**

The parameters that define the function are stored in an external memory to allow a flexible programming. The IC has three analog inputs ( $x_1, x_2, x_3$ ), and an 8-bit digital output. The output value is the result of evaluating the PWL linear function stored in the external memory at the vector point  $\mathbf{x} = (x_1, x_2, x_3)$ . Different values can be stored in the external memory, in order to program different functions.

The IC comprises two well-defined blocks: one analog, and another digital (see Fig. 3). The analog block consists of three A/D converters, based on an external ramp and a comparator based on an OTA (which has been already fabbed and tested). The digital block uses a bi-phase clock with two non-overlapping PHASES. It is designed to read the input values, retrieve the parameter data stored in the external memory and evaluate the PWL function at the evaluation point  $\mathbf{x}$  by performing a piecewise linear interpolation of the memory values. This block also generates the signals needed to read from the memory.

This approach has been implemented discretely, but the operation speed was limited to a couple of megahertz. This prototype will demonstrate the operation at higher speeds. Both blocks are powered up from different pad lines to allow them working and being tested separately.

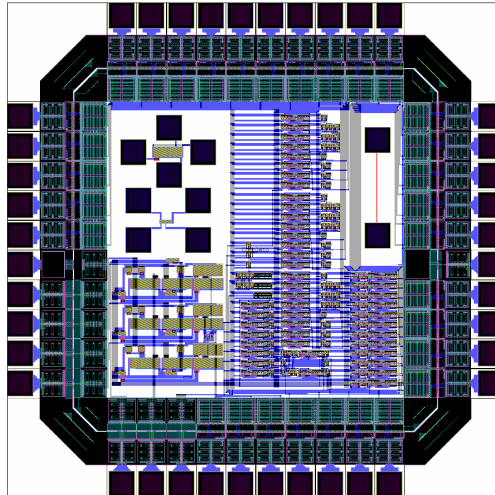


Fig. 2: Final layout of the chip.

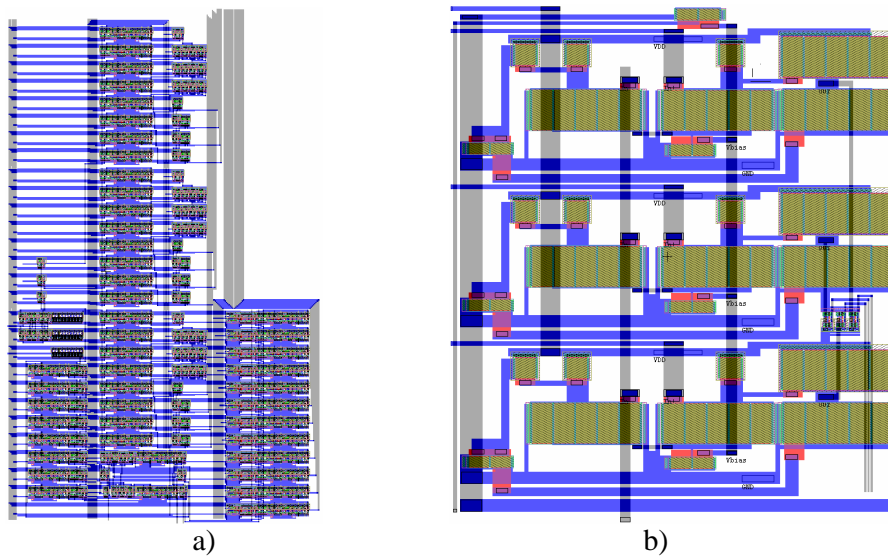


Fig. 3: a) Digital evaluation core; b) 8 bits A/D converters based on OTA.

### ***Fabrication process.***

This IC has been designed targeting the AMI 0.5 $\mu$ m process. The targeted run is that of September 6, 2005.

### ***Packaging requirements.***

The package is DIP40.

### ***Estimated project size (length and width).***

The project size is that corresponding to one (1) tiny chip in the AMI 0.5 $\mu$ m process, i.e., 2.2mm x 2.2mm.

### ***Simulation***

The simulation of the analog block was done using S-Edit. As was mentioned, this part has already been fabricated and tested in a previous design, therefore its functionality is assured.

For the digital block, a full switch level simulation using IR-SIM has been performed, which was successful.

### ***Test and characterization plans.***

After receiving the chip, it will undergo various tests to verify the correct behaviour of all its blocks. The testing of the circuit will comprise three steps:

1<sup>o</sup>) Testing of the analog block

Dissipated power, gain and bandwidth of OTA at different bias points will be checked.

2<sup>o</sup>) Testing of the digital block.

The correct evaluation of the function, the signals exchanged with the memory and the evolution of the state machine will be verified. This will be done using a setup based on a Spartan 3 (400K gates) FPGA system.

3<sup>o</sup>) Testing of the complete chip.

This final step checks the behaviour of the chip after interconnection of both blocks.

### **References**

- [1] M. Parodi, M. Storace, P. Julián, "Synthesis of multiport resistors with piecewise-linear characteristics: A mixed-signal architecture", Int. Journal on Circuit Theory and Applications, Vol. 33, No. 4, pp. 307-319, July 2005. ISSN: 0098-9886.
- [2] P. Julián, R. Dogaru, and L. O. Chua, "A piecewise-linear simplicial coupling cell for CNN gray-level image processing," IEEE Trans. Circuits Syst. I, vol. 49, pp. 904-913, July 2002.
- [3] Figueroa, JL; Cousseau, JE; de Figueiredo, RJR, "A simplicial canonical piecewise linear adaptive filter," IEEE Trans. Circuits Systems And Signal Processing, Vol. 23, No. 5, pp. 365-386, Sep-Oct 2004.
- [4] P. S. Mandolesi, P. Julian, A. G. Andreou, "A scalable and programmable simplicial CNN digital pixel processor architecture," IEEE Trans. Circuits and Systems - I: Regular Papers , Vol. 51, No. 5, pp. 988- 996, Mayo 2004. ISSN: 1057-7122.