

Proposal for: Fabricating 256x256 CMOS Polarize Imager on 10mm² die in a TSMC 0.18μm Process

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Abstract

Polarization vision contains important information about the imaged environment, such as surface shapes, curvature and material properties, which are ignored with traditional imaging systems. Several species of invertebrate, such as cuttlefish, honeybees, salmon and others, rely on contrast enhancement using polarized vision, which is of vital survival mechanism in optically scattering media. The human eye perceives visual information in terms of color and intensity and it is blind to polarization. Hence, we propose to develop a sensory system which would integrate imaging, micropolarize array and polarization processing on the same substrate. This sensor will extract polarization information in real-time using low-power translinear circuits and it will provide useful visual information to the human eye. Current polarization visual systems are composed of several bulky components, where polarization information is computed off-line by power hungry CPUs or DSPs. These set-ups are incapable of providing real-time information and they are not suitable for imaging highly dynamic environments where intensity and polarization can rapidly vary. Recent advancements in fabricating micropolarizer arrays in conjunction with our expertise in focal plane image processing architectures and polarization-related imaging techniques, will provide one of the first system-on-a-chip capable of real-time computation of polarization information in the visible regime. This bio-inspired system will be used for better target detection and visibility enhancement in underwater imaging, detection of surface deformation (e.g., fingerprint discrimination) and other applications.

Aims and Goals

The aims of the proposed research are:

- (1) to fabricate a 256 x 256 pixel CMOS image processing architecture on 10mm² die in a TSMC 0.18μm process.
- (2) to fabricate a 256 x 256 micropolarize array with pitch matched elements to the image processing sensor.
- (3) to bond the micropolarizer array on top of the image processing sensor in order to perform real-time computation of visual polarization information.
- (4) to perform various experiments in order to demonstrate the vital importance of real-time computation of polarization vision and present this information in a meaningful manner to the end user.

Significance

Extracting polarization information using low-power real-time compact sensor would require integrating imaging, micropolarize filters and processing unit on the same substrate. Previous research in this area involved systems composed of regular CMOS imagers, bulky polarization filters and off-line computation of polarization parameters. Hence, the size of such system, power hungry computation units and non-real-time computation limits the applicability of such system. We propose to develop a compact sensor capable extracting light's polarization information in real-time. The proposed sensor, which will be light-weight and portable, would be used for applications such as target detection, enhanced visibility in otherwise low-contrast conditions, longer detection range in optically scattering media, man-made polarization-sensing adaptation based on changing environments, surface deformation/variation detection (e.g., detection of finger prints on a smooth surface using polarization-based vision), "shadow removal" by displaying polarization information instead of conventional intensity information and many more novel outcomes. Our previous research has demonstrated the unprecedented capabilities in enhanced target detection using polarization difference imager [1].

Technical Approach

A. System Overview

The proposed system is based on previously developed CMOS imagers [2,3], as well as recent advancements made in the fabrication of micropolarized arrays [4,5]. The previously developed imaging architectures are the pseudo general image processor (GIP) fabricated in 1.2μm process and the linear current mode active pixel sensor with low fixed pattern noise fabricated in 0.5μm process. Both of these imaging architectures are summarized below and we outline how we propose to merge both of these systems. Various test pixels for the proposed sensor have been fabricated in 1.2μm process and initial experiments have shown promising results [6].

The GIP architecture realizes rudimentary spatiotemporal image processing at the focal plane on high resolution images using low power translinear circuits. The convolution of the incident image with programmable spatiotemporal kernels is realized with area-efficient and real-time circuits. The chip's architecture allows photoreceptor cells to be small and densely packed by performing all

analog computations on the read-out, outside the imaging array. The size, configuration and coefficients of the kernels can be varied on the fly. In addition to the raw intensity image, the chip outputs four processed images in parallel. The convolution is implemented with a digitally programmable analog processor, resulting in very low power consumption at high computation rates. A 42 by 35 pixels prototype of the GIP has been fabricated in a standard 1.2μm process and its spatiotemporal capabilities have been successfully tested. The chip exhibits 1 GOPS/mW @ 20 kfps while computing four spatiotemporal convolutions in parallel.

High fixed pattern noise associated with current mode imagers, such as the GIP, was improved with the design of the linear current mode active pixel sensor. This imaging architecture included a current domain correlated double sampling (CDS) unit for fixed pattern noise (FPN) suppression. The CDS unit is composed of first generation current conveyer circuit and class AB cascaded current memory cell. Measured FPN of 0.6% from saturation level is achieved with the CDS unit compared to 1.9% FPN from current mode images without noise suppression circuitry. A 40 by 40 imaging array was fabricated in a standard 0.5μm process and its low noise imaging functionality was successfully tested.

The proposed imaging sensor will combine the linear current mode active pixel sensor with noise suppression circuitry and analog computation units. The image processing of this sensor will be performed serially during read-out using pixel-block-parallel-addressing on the noise suppressed images. The analog computation units will be placed away from the imaging array, allowing for simple pixel circuitry which leads to high resolution imaging. Various kernels can be programmed in the analog computation units of the imager, and convolution is performed on readout with several kernels in parallel. The processing units will include: addition, subtraction, multiplication, division and squaring circuitry implemented with translinear circuits and it will further enrich the generality of spatiotemporal processing capabilities of the GIP.

Computing polarization information, i.e. extracting the Stokes parameters, is in essence a convolution computation with a 2 by 2 pixels receptive field. A micropolarizer array is placed on top of the imaging sensor with a pitch that matches the pixel filters and it contains a 2 by 2 pattern which is replicated across the micropolarizer array. Hence, a neighborhood of 2 by 2 pixels will be accessed in parallel and each pixel will be scaled accordingly to the Stokes parametric equations. The micropolarizer array will be fabricated at the University of Pennsylvania micro fabrication facilities using approaches described in [4] and [5]. The pixel pitch of the micropolarizer array will match the 10μm pitch of the imaging sensor.

B. Chip Overview

The three main components of the imaging sensor are: (1) 256 rows by 256 columns photo pixel array; (2) three vertical and three horizontal scanning registers and (3) a single processing unit (see Figure 1). The three vertical and three horizontal scanning registers select several groups of single or multiple pixels within a given neighborhood of the photo array. The linearly amplified photocurrent values of the selected pixels are then passed to the processing unit, where noise cancellation and convolutions with the desired filter are computed. The processing unit, which consists of four identical but independent sub-processors, is implemented with digitally controlled analog multipliers and adders. The multipliers and adders scale each of the pixel photocurrents according to the convolution kernel being implemented. The final output of the processing unit is a sum of scaled photocurrents from the selected neighborhood. The independent groups of pixels can be combined in various ways, allowing for the realization of various complicated separable or non-separable filters, as well as the computation of Stokes parameters of the polarized light. Each of the four sub processors can be independently programmed in parallel, allowing for three of the Stokes parameters to be computed simultaneously as well as an intensity image to be presented to the output of the chip.

The photo pixel (see Figure 2) is composed of a photo diode, a reset transistor (M1) and three transconductance amplifiers (M2, M3 and M4 transistors), which output three amplified photocurrents. The photodiode, implemented with N-diffusion and P-substrate, is connected to a reset transistor M1, which controls the operation modes of the photodiode. The linear photo pixel in the later design operates from two separate power supplies which enable transistors M2, M3 and M4 to operate in the linear region. Hence linear conversion from light intensity to output amplified current is achieved.

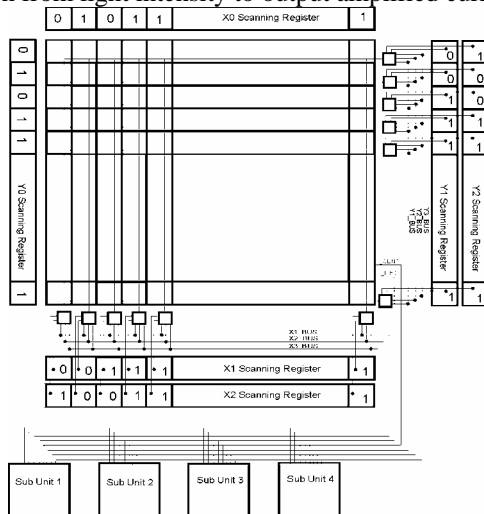


Figure 1: Block diagram of the chip.

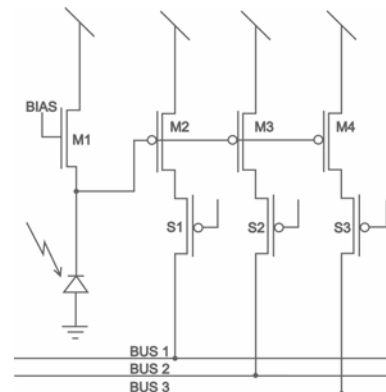


Figure 2: Pixel Schematic

C. Results from a the GIP and Linear Current Mode Pixel Prototype

Figure 3 shows examples of the GIP outputs when the incident image is convolved with various 5 x 5 kernels. Four parallel images were obtained, each using a different kernel. The top row images are the intensity, horizontal and vertical 1D Laplacian edge images, respectively. The second row images are the 45-degree, 135-degree and 2D Laplacian edge images. The third row images are Gaussian, 2D diagonal edge detection and 2D edge detectors with the diagonal edges suppressed. Due to larger kernel size, some smoothing effects are observed in the convolved images.

The fixed pattern noise of the linear current mode imager is evaluated with and without the CDS unit. The fixed pattern noise with noise suppression circuitry is 0.6% of the saturation current and it is comparable to the fixed pattern noise off-the-shelf digital imagers. This error is primarily due to charge injection errors in the current memory cell and hole mobility dependence on vertical electric field under the gate of transistor M2, which can be further improved. The fixed pattern noise without noise suppression circuit is 1.9% of saturation current and it is largely due to the threshold voltage variations of the transimpedance amplifier M2, M3 and M4.

Real life images obtained with this imager are presented in Figure 4, where the benefits of the current mode CDS are evident. The left image is obtained using noise correction circuit and it presents smaller variations between pixels with similar intensity. The image on the right is obtained without noise correction and larger variations between pixels with similar intensity (background and facial skin) are easily observed.

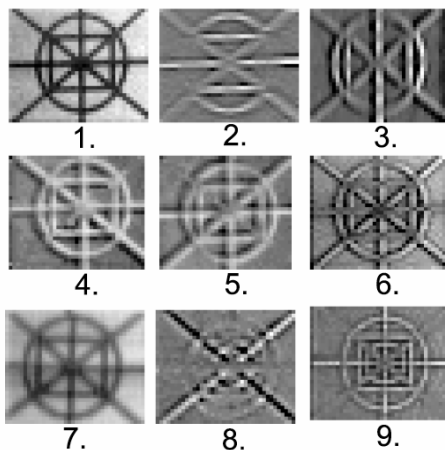


Figure 3: Convolved images with 5x5 mask size: 1. Intensity Images; 2. Horizontal Edges; 3. Vertical Edges; 4. 45.Degree Edges; 5. 135 Degree Edges; 6. Laplacian Edges; 7. Gauss Smoothing; 8. Diagonal Edges; 9. Vertical-Horizontal Edges.

Figure 4: Real life images with CDS (left) and without (right) CDS correction

References

- [1] E. N. Pugh, Jr., N. Engheta, M. P. Rowe, and J. S. Tyo, U.S. Patent Number # 5,975,702, "Method of Using Polarization Differencing to Improve Vision", November 2, 1999.
- [2] V. Gruev and R. Etienne-Cummings, "Implementation of Steerable Spatiotemporal Image Filters on the Focal Plane," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, pp. 435-440, 2002.
- [3] V. Gruev, R. Etienne-Cummings and T. K. Horiuchi, "Linear Current Mode Imager with Low Fix Pattern Noise," *IEEE ISCAS 2004*, 2004.
- [4] J. Guo and D. Brady, "Fabrication of thin-film micropolarizer arrays for visible imaging polarimetry," *Applied Optics*, Vol. 39, No. 10, 2000.
- [5] S.-C. A. Lien, P. Chaudhari, J. A. Lacey, R. A. John and J. L. Speodell, "Active-matrix display using ion-beam-processed polyimide film for liquid crystal alignment," *IBM Journal of Research and Development*, Vol. 42, No. 3/4, 1998.
- [6] V. Gruev "VLSI Implementation of Steerable Spatiotemporal Filters for Focal-Plane Adaptive Image Processing," *PhD dissertation thesis*, 2004.

Estimated project size

The estimated project size is:

- (1) die size of the chip will be 10mm².
- (2) the chip will be packaged in PGA84M.
- (3) the chip will be fabricated TSMC 0.18μm process.

The total cost for fabricating and packaging 40 chips will be \$32,400. In order to effectively use this imaging system to study polarization of light, the imager must satisfy two requirements: 10μ pixel pitch and 256x256 photo array. This will bound fabrication of 10mm² chip in a TSMC 0.18μm process. Two prototype versions of current mode image processing architectures were designed, fabricated and tested in HP 0.5μm and AMI 1.2μm process. These imaging chips achieved low-power and low-noise imaging and

pseudo general visual processing in the focal plane. Test pixels of the proposed sensors have been successfully fabricated and tested in HP 0.5 μ m and a fabrication of a complete sensor is proposed.

Simulation plans and Testing Plans

The imaging system is designed using Cadence Design tools. All analog circuits have been simulated using Spectra Spice, while the digital circuits have been simulated using VerilogXL and Spectra simulations. The prototypes of this imaging system were tested extensively and results have been published [2,3,6]. The new imaging sensor will be integrated with Scenix microcontroller, which controls all the digital circuitry in the imager and synchronizes the readout of each image frame with high speed National Instrument 6533 DIO card into the PC. High speed, low noise 12 bit ADC board has been design as part of the testing bench, which is used to digitize and characterize the image quality. Testing of the imager will involve: characterizing the signal to noise ratio, matching characteristics of transistors, measuring dark current of the photo diode, measuring photo response of the photo diode, measuring fixed pattern noise in the image, measuring the computational speed of the analog subtraction circuitry and characterizing the operational amplifier. Also, small feature size will be applied for designing this imager and this will be characterized and compared with previous imaging designs. Real time software for displaying images has been developed and used for the pervious prototype. The final step of this project will be to successfully integrate the imaging sensor with micropolarize array filters for real-time computation of visual polarization. This would allow us to explore the potential integration of fast focal plane CMOS image processor with micropolarizer array for better target detection and visibility enhancement in underwater imaging, detection of surface deformation (e.g., fingerprint discrimination) and other applications.