

A 60-GHz Double-Balanced Gilbert Cell Down-Conversion Mixer on 130-nm CMOS

Fan Zhang, Efstratios Skafidas, William Shieh

National ICT Australia, Department of Electrical and Electronic Engineering,
The University of Melbourne, VIC 3010, Australia

Emails: f.zhang@ee.unimelb.edu.au, stan.skafidas@nicta.com.au, w.shieh@ee.unimelb.edu.au

Abstract—Homodyne receiver structures enable low cost integrated transceivers. A critical requirement of these systems is a high isolation mixer. In this paper, a high LO to RF isolation, double-balanced (Gilbert Cell) 60-GHz down-conversion mixer is presented. This mixer achieves a voltage conversion gain better than 2 dB, input-referred IP3 point of -8 dBm and LO to RF isolation greater than -36 dB when driven with a LO input of 0 dBm.

Index Terms—millimeter wave circuit, Gilbert-Cell mixer, RF CMOS, 60-GHz band, down-conversion.

I. INTRODUCTION

High frequency and even millimeter wave analog communication circuits, which were traditionally built on more expensive technologies such as bipolar or Gallium Arsenide (GaAs), are gradually being implemented on CMOS [1][2].

In order to facilitate cost effective transceivers, designers pursue homodyne receiver architectures. An important consideration in homodyne receiver structures is LO to RF isolation of the mixer. LO self-mixing [3], occurs when the LO signal (which is the same frequency as the RF signal) leaks to the input of the mixer and then mixes with itself. This self-mixing produces DC offset which significantly degrade the receiver's performance. In the literature, very few results have been presented for mixers which are suitable for homodyne architectures, operating at the 60-GHz frequency range. In this paper a high LO to RF isolation mixer is presented that enables a 60-GHz direct-conversion (homodyne) receiver. This work contains design procedures and measurement results for a 60-GHz double-balanced Gilbert Cell down-conversion mixer with improved LO to RF isolation and nonlinearity.

The paper is organized as follows. Section II provides of methodology for transistor sizing to optimize f_{max} and NF_{min} . In Section III, an analysis of a Gilbert-Cell Mixer structure is performed. Conversion gain, matching networks and noise figure minimization of the mixer are investigated. Layout recommendations are also provided in this section. Section IV presents the measurement results of voltage conversion gain, linearity and LO to RF isolation of the mixer with on-chip Balun fabricated using the methodology. The results of this mixer are compared to other mixers reported in the literature.

II. TRANSISTOR DESIGN CONSIDERATIONS

The first step in the design of the mixer is determining the appropriate size of transistors and their layout to trade off cor-

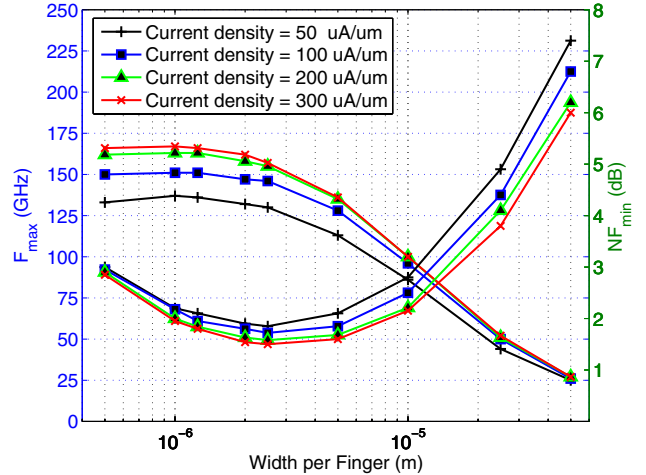


Fig. 1. f_{max} and NF_{min} of a Transistor, Total Width = $50 \mu\text{m}$, Current Density = $50 \mu\text{A}/\mu\text{m} \sim 300 \mu\text{A}/\mu\text{m}$, Finger Width = $0.5 \mu\text{m} \sim 50 \mu\text{m}$.

responding gain and noise figure. One of the most commonly used figure-of-merit of a process is the maximum frequency of oscillation (f_{max}). This is defined as the frequency at which the extrapolated power gain falls to unity. The value of f_{max} is determined by sizing, bias conditions as well as transistor resistive loss and layout parasitics [1].

In order to find the optimum finger width for the mixer's transistors, varying finger width transistors in common source configuration was simulated. In this procedure, we simulated transistors of fixed total width and varied the number of transistor fingers and run multiple simulations for each simulation the current density was fixed. The aim was to determine the relationship between finger width and f_{max} and NF_{min} .

The mixer is fabricated on IBM CMOS8RF technology. This technology is a 130-nm CMOS technology with 8 metal layers, 3 thin, 2 thick copper layers and 3 RF layers. Fig.1 shows the simulation results of f_{max} of this technology. All of the simulations are of the same total width ($50 \mu\text{m}$) transistor. The current density varies from $50 \mu\text{A}/\mu\text{m}$ to $300 \mu\text{A}/\mu\text{m}$ and the width per finger varies from $0.5 \mu\text{m}$ to $50 \mu\text{m}$. By using narrow finger width, the effect of the gate resistance can be made negligible compared to the other parasitic resistors [1]. However, when the finger width is decreased (below $1 \mu\text{m}$), no obvious improvement for f_{max} is observed. This phenomenon

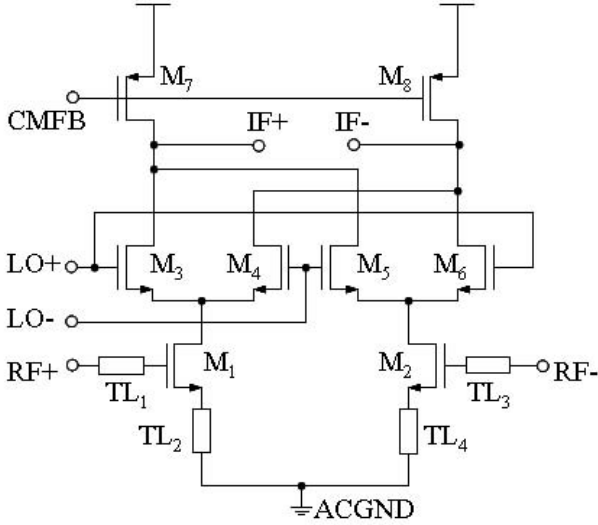


Fig. 2. Simplified schematic of double-balanced mixer core. Biasing circuits have been omitted for clarity.

differs from what is reported in [1]. For certain current density, the f_{max} degrades further. From Fig.1, it can be seen that the maximum f_{max} can be obtained where finger width is between 1 and 5 μm . By choosing proper finger size and biasing, the f_{max} can reach 150 GHz. More over, the device must be biased well into strong inversion (around 100~300 $\mu\text{A}/\mu\text{m}$) for highest f_{max} .

Another important consideration is minimum noise figure (NF_{min}) and its relationship to finger width. This has been plotted in Fig.1. The NF_{min} was calculated for 60 GHz operation. As has been reported in the literature, it can be seen that finger width can not be simultaneously optimized for both NF_{min} and f_{max} . One needs to determine optimal finger width by trading off NF_{min} and f_{max} . For optimal operation utilizing IBM CMOS8RF process, the finger width should be in the range from 1 to 4 μm since both the NF_{min} and f_{max} are minimized and maximized within this range.

III. MIXER DESIGN

In order to achieve better noise figure performance and higher SNR for the whole system, the receiver front end of 60 GHz transceiver is chosen to be differential, which requires the mixer to be able to handle differential inputs. The double-balanced structure in Fig.2 provides better LO to RF isolation compared to other single gate mixers [4] or single balanced mixers [2]. This is critical for direct down conversion systems. In direct down conversion receivers, the LO and input signals are identical in frequency. The leakage of LO signal to RF port will mix with itself and cause DC offset at the IF port. Therefore LO to RF isolation is crucial for the successful performance of a whole receiver. Subsequently, the double-balanced structures that perform cancellation of the unwanted signals are used in this mixer design.

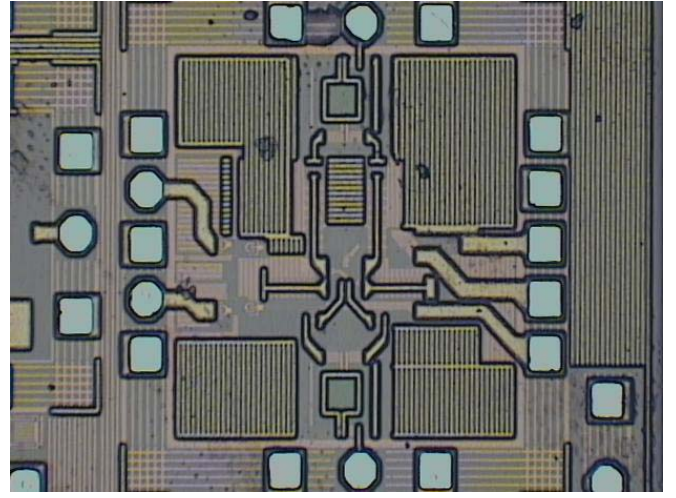


Fig. 3. Mixer with two on-chip transformer Baluns (900 $\mu\text{m} \times 900 \mu\text{m}$)

A. Matching Networks

Fig.2 shows simplified schematic of a double-balanced mixer. TL_2 and TL_4 are two microstrip lines serving as source degeneration inductors and TL_1 and TL_3 are implemented to match the differential inputs to 50 Ω .

The input impedance looking into the transconductance stage is:

$$\begin{aligned} Z_{in} &= j\omega L_{TL_2} + \frac{1}{j\omega C_{gs}} + \frac{g_m L_{TL_2}}{C_{gs}} + j\omega L_{TL_1} \\ &= j\omega L_{TL_2} + \frac{1}{j\omega C_{gs}} + \omega_T L_{TL_2} + j\omega L_{TL_1} \quad (1) \end{aligned}$$

For a given transistor, C_{gs} is determined by the physical layout of M_1 , so by adjusting L_{TL_2} and L_{TL_1} , theoretically, we can get the impedance matched to 50 Ω for all different sized M_1 . It also can be shown that the inductive degeneration increased linearity without raising the noise. More over, by choosing a certain number of fingers, we have a control over C_{gs} of M_1 and with certain L_{TL_2} and L_{TL_1} the NF_{min} can be achieved with input port still matched.

B. Active Loads

The load used in this Gilbert Cell mixer is a pair of PFET transistors. They were chosen in order to achieve sufficient bandwidth and gain with the limited voltage headroom available. In order to get higher r_O , non-minimum length of PFETs have been used and the PFET transistors are biased into strong inversion region.

However, in order to drive a fixed amount of current, the longer the channel, the wider the width required, which may cause the PFET to be too large (since μ_p is about 1/4 of μ_n).

C. Noise Figure Consideration

The noise of double-balanced mixer primarily comes from the transconductance stages and switching pairs. The analysis for a matched transconductance stage, such as the one used in this design, has been done in [5] and [6].

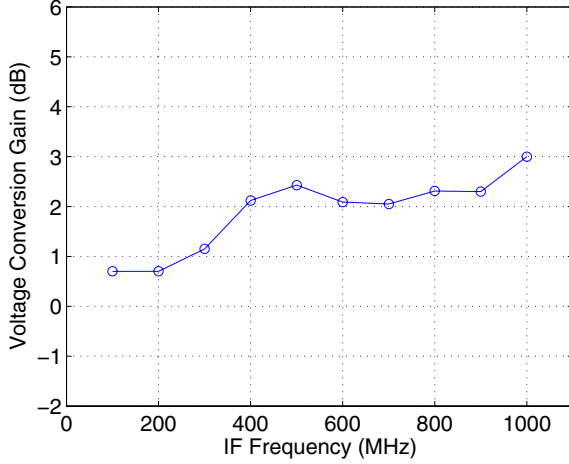


Fig. 4. Voltage conversion gain variation in a channel

The noise figure of the transconductance is:

$$NF_{transc} = 1 + \frac{\omega^2 L_s^2}{\omega_T} \left[\gamma g_{d0} + \frac{\delta}{5g_{d0}} \left(\frac{1}{\omega^2 L_s^2} + g_m^2 \right) - 0.79g_m \sqrt{\frac{\gamma\delta}{5}} \right] \quad (2)$$

where $\omega_T \approx g_m/C_{gs}$ is the transit frequency of transistor, g_m is transconductance of transistor, γ is the excess noise-factor of transistor, δ is the gate-noise coefficient and g_{d0} is the zero-bias drain conductance.

In this design we followed the following guidelines to minimize the noise from the transconductance stages [6]: 1) maximize the unity gain frequency of transistors and bias the devices at high enough current densities and, 2) pick a degeneration inductor that gives a feedback factor $g_m\omega L_s$ approximately equal to 0.5.

The switching pairs exhibit imperfect switching which attenuates the RF signal. Their simultaneous conduction magnifies the noise from the LO which degrades the noise figure of the mixer. Hence to improve mixer performance sufficient LO drive and appropriate biasing must be supplied to make the differential pair behave closer to an ideal switching pair. In this design, the switching pair was designed to be driven by an LO power of 0 dBm.

D. Layout Considerations

Because of the short wavelength of 60 GHz special considerations must be given to make the circuit as symmetrical as possible in layout to maintain balance between signals. Transmission line crossings as well as differences between path lengths increase the unbalance which reduced the isolation between ports.

In this design, microstrip lines were used to implement the degeneration impedance, matching networks and transmission lines. Microstrip lines on silicon are typically implemented using the top-layer metal as the signal line, and the bottom-layer metal for the ground plane.

Though using top-layer signal line and bottom-layer ground plane can give us more inductance for the same dimensions, it

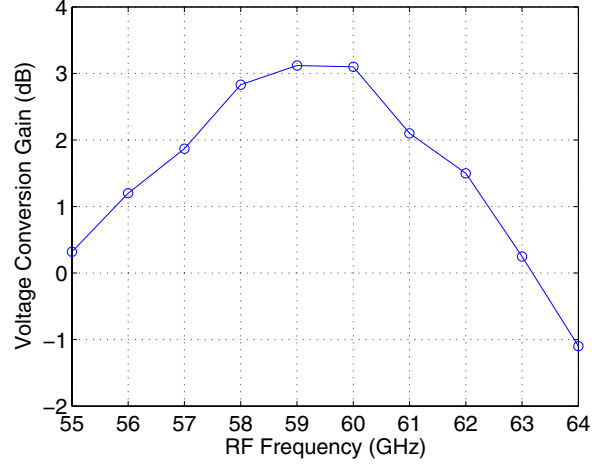


Fig. 5. Voltage conversion gain Vs RF frequency.

also leads to a much more complex mixer layout. With such a complex layout, a feed through path could be easily generated from LO to RF. Since the LO signal is very strong in mixer and undesirable for direct conversion receiver structure [7], it needs to be minimized. More over, through the simulation, a 5 dB higher Q value was observed when using higher layer ground plane. In this design, to minimize the chance of feed through, higher layer (specifically MG and MQ) ground planes were used.

IV. MEASURED RESULTS

The mixer design was fabricated on the IBM 0.13- μm CMOS8RF technology using 8-metal layers. An output buffer consisting of two source followers has been implemented in order to drive 50- Ω load when doing measurements. Since the buffer used in this design does not provide any gain, the measured results presented in this section reflects the mixer's intrinsic performance. Two transformer Baluns (single-ended to differential) were built on-chip at the RF and LO port in order to make differential measurements.

The die photo of the fabricated mixer is shown in Fig.3. With two baluns and testing pads, the layout of mixer occupies an area of 900 $\mu\text{m} \times 900 \mu\text{m}$. The mixer was measured using Suss-Microtech Probe Station with 110-GHz probes and a 110-GHz Anritsu Vector Network Analyser.

Fig.5 and Fig.4 depict the measured voltage conversion gain variation across all the frequency band and within an OFDM sub-channels respectively. For Fig.5, IF frequency was set to be 1 GHz by adjusting LO frequency to the correspondent values(1 GHz lower than RF frequency) when changing RF input frequency. In measuring the gain variation of a sub-channel, as shown in Fig.4, RF input frequency varies from 59.1 GHz to 60 GHz with fixed LO frequency of 59 GHz and hence IF frequency varies from 100 MHz to 900 MHz. The de-embedded power gain was translated to correspondent voltage gain for the down-conversion mixer.

The measured LO to RF isolation performance is shown

TABLE I

SUMMARY OF THE MIXER PERFORMANCE COMPARED WITH OTHER RECENT MM-WAVE MIXERS

Ref.	RF freq.(GHz)	Technology	Architecture	Gain(dB)	P1dB(dBm)	IIP3(dBm)	LO to RF Isolation(dB)
This work	60	130-nm CMOS	Gilbert Cell	2	-15	-8	-36
[4]	60	130-nm CMOS	Single FET	-2	-3.5	N/A	-12
[2]	60	130-nm CMOS	Single Balanced	28	-22.5	N/A	N/A
[8]	20	80 GHz f_t SiGe	Gilbert Cell	10	-21	-11.3	N/A

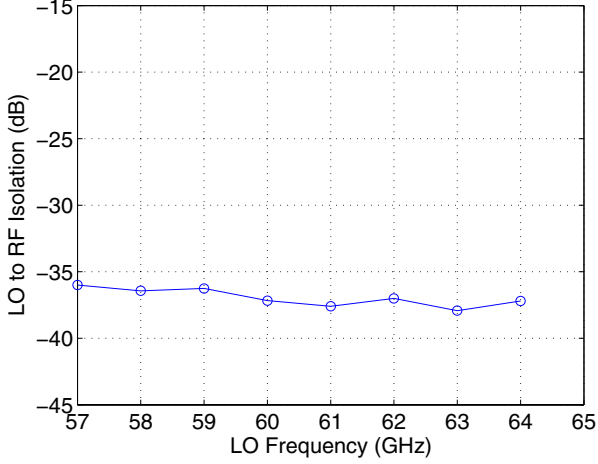


Fig. 6. LO to RF isolation

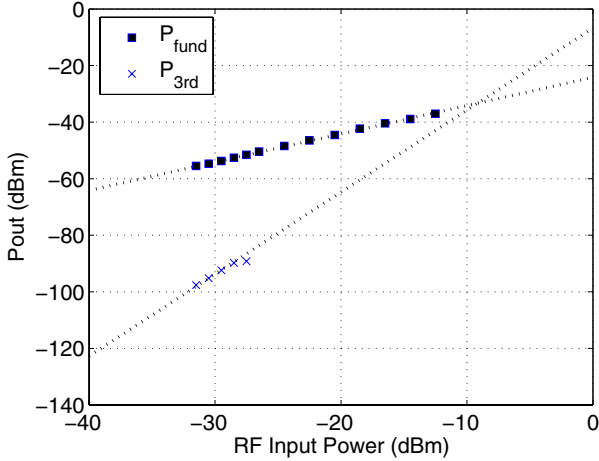


Fig. 7. P1dB and IIP3

in Fig.6. In the frequency band from 57 GHz to 64 GHz, an isolation of better than -36 dB was achieved. This was attributed to the cancellation of LO signal at RF port due to the double-balanced mixer structure. An even better isolation is possible by making the mixer layout more symmetric. The input third-order intercept point (IIP3) is illustrated in Fig.7 and two RF tones(one at 60.0 GHz and the other 59.9 GHz) have been combined through a power divider and fed into the the mixer. With a 59.5-GHz 0-dBm LO drive, the measured IIP3 point is -8 dBm and P1dB is -15 dBm. Since the

designed mixer is designed to operating with a 1.2-V supply voltage, the linearity can be further improved when higher supply voltage is applied.

The summarized performance of the mixer is in Table.I along with other published mm-wave mixers (IP3 and P1dB compression points for [8] are output-referred). It's important to note that IF amplifiers were included in some of these mixers to provide higher gain.

V. CONCLUSION

An important component in enabling low cost homodyne receivers on CMOS is mixers with high LO to RF isolation. In this paper methods to develop such a mixer are presented. Furthermore a double-balanced down-conversion mixer has been designed and fabricated on IBM 130-nm CMOS technology for direct conversion receiver operating at 60-GHz band. For RF input signal of 60 GHz, with 0-dBm LO power, a conversion gain of 2 dB has been measured. The measured IIP3 point is -8 dBm and P1dB is -15 dBm.

VI. ACKNOWLEDGMENT

This work was funded by National ICT Australia (NICTA) Victoria Research Laboratory. The authors wish to thank G.Felic for her design of on-chip transformer Balun and the whole 60-GHz RF design group for useful discussion. The authors also wish to thank MOSIS and IBM for providing foundry access.

REFERENCES

- [1] C.H.Doan, S.Emami, A.M.Niknejad, and R.W.Brodersen, "Millimeter-wave CMOS design," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 144 – 155, Jan. 2005.
- [2] B.Razavi, "A 60-GHz CMOS receiver front-end," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 17 – 22, Jan. 2006.
- [3] T.H.Lee, *The Design of CMOS Radio-Frequency Integrated Circuit*. Cambridge University Press, 2004, 2nd Edition.
- [4] S.Emami, C.H.Doan, A.M.Niknejad, and R.W.Brodersen, "A 60-GHz down-converting CMOS single-gate mixer," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 163 – 166, June 2005.
- [5] M.T.Terrovitis and R.G.Meyer, "Noise in current-commutating CMOS mixers," *IEEE J. Solid-State Circuits*, vol. 34, no. 6, pp. 1399 – 1410, June 1999.
- [6] M.T.Terrovitis, "Analysis and design of current-commutating CMOS mixers," Ph.D. dissertation, University of California, Berkeley, 2002.
- [7] A.Abidi, "Direct-conversion radio transceivers for digital communications," *IEEE J. Solid-State Circuits*, vol. 30, no. 12, pp. 1399 – 1410, Dec. 1995.
- [8] S.Hackl, M.Wurzer, J.Bock, T.F.Meister, H.Knapp, K.Aufinger, L.Treitinger, and A.L.Scholtz, "Benefits of SiGe over silicon bipolar technology for broadband mixers with bandwidth above 10 GHz," *2001 IEEE MIT-S International Microwave Symposium Digest*, vol. 3, pp. 1693 – 1696, May 2001.