

**Design for MOSIS Educational Program (Research)**  
**An Adaptive Cross-Correlation Derivative Algorithm for Ultra-Low Power  
Time Delay Measurement**

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# Proposal for MEP Research Program:

## An Adaptive Cross-Correlation Derivative Algorithm for Ultra-Low Power Time Delay Measurement

### ***Project description.***

#### A. INTRODUCTION

The objective of this proposal is to fabricate an integrated circuit that implements an adaptive cross-correlation technique for the measurement of the interaural time delay (ITD) between two signals.

Several techniques such as Independent Component Analysis, Cross-correlation analysis [1],[10], Gradient Flow techniques [14], and the emulation of the human hearing cochlea [10], [4], [15], can be used for the localization of acoustic sources. Indeed, a number of analog and digital VLSI circuits have been successfully demonstrated in [10] [4][2][3][15], yet only a few of them have been designed to satisfy power consumption restrictions. Van Schaik and Shamma [15] reported an integrated circuit (IC) based on the analog model of a human cochlea with a power dissipation that varies between 400  $\mu$ W and 1.85 mW depending on the input signal. Stanacevic and Cauwenberghs [14] proposed the analog processing of a signal at a sampling rate of 16 kHz, which can discriminate delay differences down to 2  $\mu$ s, with a power consumption of 32  $\mu$ W. Several realizations based on the cross-correlation derivative algorithm as proposed in [5] are reported in [6] and [8]. This method is a variation of the measurement of the ITD, which reduces the complexity of the calculations, and therefore is well suited for low power operation. The version presented in [8] is a 1.5mm  $\times$  3mm IC fabricated on a standard 0.5 $\mu$ m CMOS process that can discriminate delay differences down to 5 $\mu$ s with a power consumption of 12 $\mu$ W at 2V.

We intend to fabricate an integrated circuit –in the TSMC 0.35 $\mu$ m process– that implements an alternative realization for the cross-correlation algorithm that reduces power consumption still further, while keeping calculation performance. The cross-correlation derivative (CCD) approach is a variation of the standard time-domain cross-correlation between two signals. The CCD algorithm works with a one bit discrete quantization of the input signals, and therefore, reduces drastically the complexity of the resulting digital circuitry. Another feature is that the spatial derivative of the cross-correlation is calculated instead of the cross-correlation itself. Calculation of the CCD results in an activity reduction of a thousand times in the digital circuitry. In the case of the standard cross-correlation approach, once the partial correlations are calculated, the maximum needs to be evaluated which requires a dedicated stage. In the CCD, it is only necessary to locate a change in the output value of the partial correlations (which are either 1 or 0), making this task trivial: one only needs to detect transitions of the input signals. The strategy proposed in this chip is the use of a single counter for delay measurement together with an adaptive closed loop system. The closed loop guarantees stability, and also a convergence of the counter count to the delay under measurement. The reduction of power consumption is a consequence of the reduction in size of the circuitry. In fact, just one counter for the whole IC is needed as opposed to the previous versions [6] and [8] where one counter per delay tab was needed.

#### B. STRUCTURAL DESIGN (FRONT-END)

The first objective is to obtain the same accuracy as in previous CCD implementations. The front-end design was coded using Verilog HDL and the Xilinx® Integrated Software Environment (ISE) and implemented on a Spartan3 Digilent Inc. prototyping board. Simulations were run on Mentor Graphics® ModelSim® HDL simulator. Simulations were run at the RTL and gate level. Results from the ModelSim® simulator were fed into Matlab® for a preliminary accuracy check.

Figure 12 depicts the basic structure, composed of a block that captures and stores the signals being measured, and a second block which calculates the delay. The output has a tri-state control (oe\_L) to allow its interfacing to a general data bus, with two extra signals providing information about the state of the unit, i.e., if it is out of its measurement range (out\_range) and if data is available (data\_rdy).

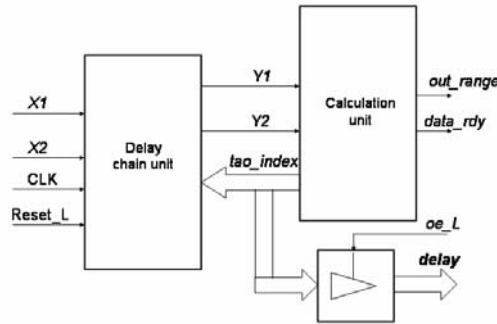


Figure 1. Block diagram of front-end design

### C. DELAY CHAINS

The first block, shown in Fig. 3, captures the signals at a 200 kHz rate. This rate was fixed due to previous design constraints [5]. Data is stored in two Serial In-Parallel Out registers that serve as delay chains. Considering such speeds, the circuit proposed would allow for the measurements of  $\pm 640 \mu\text{s}$  of delay.

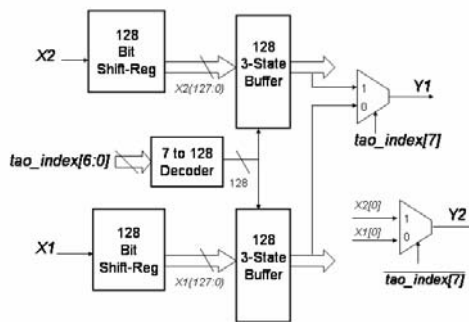


Figure 2. Block diagram of the delay chain

Registers and multiplexers are generated using Verilog's generic parameters so as to speed up post placement simulation times. This simulation and description benefits are used keeping in mind that in the VLSI implementation particular care must be taken to build these blocks.

For reference's sake, it is always assumed that signal X1 leads X2. The first bit of one of the chains (by convention X2) is used as base pointer, while the other chain is swept in search of transitions by the signal tao\_index. This index is an 8-bit signed integer in two's complement. The sign bit switches the multiplexers in the case where X1 is actually lagging

X2, instead of leading it. Thus, the base pointer is switched to X1[0] and the index's magnitude is used to sweep X2.

#### D. CALCULATION UNIT

The calculation unit must discover valid transitions in the input signal to account for an increase or decrease of the index counter, depending on the index sign bit. Repeated application of the calculation will produce a monotonic estimation of the target delay. Since the circuit is designed to increase or decrease its count by one on each valid transition, the convergence time is determined by:

$$T_{convergence} = \frac{1}{2} * \frac{f_{CLK}}{f_{signal}} * |Delay_{current} - Delay_{new}| \quad (1)$$

where  $|Delay_{current} - Delay_{new}|$  is the absolute signal delay change from a steady state measurement to the new value of delay to measure, that is, the difference between the current delay and the delay value that the system has to reach. An out\_range signal is provided to indicate the saturation of the index counter. This serves as an auxiliary signal to allow for the adaptive measurement of faster or slower signals via the modification of the clock speed.

Boolean equations for the control of the delay counter, DN\_UP and CNT\_CLK were obtained using Berkeley's Espresso minimization algorithm and were tested on the FPGA by directly introducing them into the RTL code instead of the high level decision sentences used in the original front-end implementation.

$$DN_{UP} = \overline{SGN} * (A + B) + \overline{SGN} * \overline{OVN} * (C + D) \quad (2)$$

$$CLK_{CNT} = \overline{SGN} * \overline{OVN} * (C + D) + SGN * \overline{OVN} * (C + D) + (A + B) \quad (3)$$

$$A + B = \overline{Y_1} * Y_{1\_K1} * \overline{Y_2} * \overline{Y_{2\_K1}} + Y_1 * \overline{Y_{1\_K1}} * Y_2 * Y_{2\_K1} \quad (4)$$

$$C + D = \overline{Y_1} * Y_{1\_K1} * Y_2 * Y_{2\_K1} + Y_1 * \overline{Y_{1\_K1}} * \overline{Y_2} * \overline{Y_{2\_K1}} \quad (5)$$

For the validation of the transitions, the signals pass through two registers. The decision logic determines whether to increase, decrease or leave the counter unchanged depending on the arrival order of the transitions and variable tao\_index current state. Transitions are checked on the rising and falling edges of the input signals. Evaluation thus occurs at a speed twice as fast as the signal's frequency (on a noise-free signal). The decision logic is registered in order to eliminate the chance of falsely locking the circuit to the same transition. This avoids a run-up in the counter.

#### OTHER STRUCTURES

In order to fully exploit the availability of the run in this process, several sub-units will be included for testing purposes, using a separate set of pads. One of them will be two digital delay chains, one using C2MOS registers, and the other using Static CMOS registers. Another will include the calculation unit without the delays chains; this unit, in conjunction with an external FPGA will allow us to implement variations of the algorithm using the same Silicon structure. Another block will contain test structures at the transistor level, including different size transistors and gates.

### **Fabrication process.**

This IC has been designed targeting the TSMC 0.35  $\mu\text{m}$  process. The targeted run is that of March 5, 2007.

## ***Packaging requirements.***

The selected package is PGA 65. A total of 12 parts will be requested to be packaged, and the remaining in dies.

## ***Estimated project size (length and width).***

The project size is 2.3mm x 2.3mm in the TSMC 0.35 $\mu$ m process.

## ***Simulation***

The design of the chip followed these steps: high level design using Verilog HDL, high level simulation, RTL level simulation, FPGA functional verification, post-layout simulation. At every stage of the design, simulations were performed using a set of test signals designed in Matlab that played the role of the Gold Reference Model.

### A. FUNCTIONAL SIMULATION AND FPGA TESTING

Simulations were run at the RTL level and the gate level (with back annotation from the post placement and routing models written by ISE®). Results from the ModelSim® simulator were fed into Matlab® for a preliminary check of the accuracy of the method. A set of files with test signals was created in Matlab® to serve as stimulus signals to the simulator.

### B. VLSI REALIZATION

A schematic based on the logical Verilog design was drawn on Tanner® S-Edit, including all the constraints regarding power consumption. Based on this schematic, a handcraft layout of the circuit was drawn on Tanner® L-Edit, from which a SPICE model was extracted for its simulation on Mentor Graphics® Eldo and Mach-TA for analog timing checking, power estimations and digital verification. Considering its size and operational speed, the Delay Chain unit is the responsible for the maximum power dissipation. In order to minimize power consumption, the SIPO delay chains were built using eight transistor C2MOS registers. This master-slave edged triggered register does not need feedback, as the data is stored in the internal node capacitances, and features a lower clock fan-in and a smaller area compared with the eighteen transistors required for a static register [11].

## ***Test and characterization plans.***

A testbench for the functional verification of the IC was written in Verilog HDL and implemented on a Digilent Inc. Spartan 3 Board. The system is able to generate different delays between two reference 200 Hz signals. Both delayed signals are supplied by a programmable delay generator with a step size of 2.5 $\mu$ s. The delays are either pre-programmed using a look-up table or taken from the pseudo-random sequential vectors provided by a LFSR register. The different delays are sequentially and asynchronously fed to the IC at a time rate of 1 second per vector. This allows for full convergence of the IC to a steady state. The IC output bus is read at a 1.25ms sampling rate, and gives a long enough interval for the measurement of at least 200 samples of the target delay estimation in steady state. Data is taken from the testing board and fed to a PC with Matlab via RS-232.

This test workbench has already been built and tested with the FPGA realization of the chip. Power consumption will be measured in idle mode, and in operation mode using a Pico-ammeter.

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