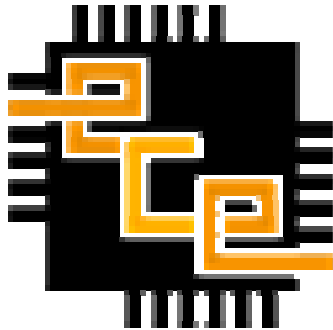


**Design for MOSIS Educational Program (Research Proposal)**

**Proposal for chip fabrication by Purdue University for the 2007  
calendar year**



**ELECTRICAL AND  
COMPUTER ENGINEERING  
PURDUE UNIVERSITY**

**Prepared by:**

Ruilin Wang (Grad Student) and Cheng-Kok Koh (Professor),  
Sanghoon Joo (Grad Student), Mac Inerowicz (Grad Student), Charles Chen (Grad Student)  
and Byunghoo Jung (Professor),

Jaydeep P. Kulkarni (Grad Student), Sang Phill Park (Grad Student) and Kaushik Roy  
(Professor),

Hanil Lee (Grad Student) and Saeed Mohammadi (Professor)

**Institution:** School of Electrical and Computer Engineering,  
Purdue University

**Date of submission:** May 8, 2007

## Summery

This proposal is requesting funding for the fabrication of a chip which is composed of 4 different designs for research purpose by Purdue University for the 2007 calendar year. The total area requested is  $4\text{ mm} \times 4\text{ mm}$ . The designs and their area requirements are summarized in the following:

**Design 1:** An improved 10GHz R<sup>2</sup>TWO distributed oscillator for low-power, low-skew and low-jitter global clock generation/distribution. The area requirement is  $2\text{ mm} \times 2.5\text{ mm}$ .

**Design 2:** A low-noise amplifier and a power amplifier. The area requirement is  $2\text{ mm} \times 2\text{ mm}$ .

**Design 3:** A variation-resilient PLL and SRAM. The area requirement is  $2\text{ mm} \times 2\text{ mm}$ .

**Design 4:** A programmable RF matching network. The area requirement is  $2\text{ mm} \times 1.5\text{ mm}$ .

### **Proposed Design**

See individual proposals.

### **Fabrication Process**

IBM 8RF-DM 0.13um CMOS

### **Anticipated Design Size**

$4\text{mm} \times 4\text{mm}$

### **Packaging Requirements:**

Some test chips will be packaged.

### **Simulation Plans**

See individual proposals.

### **Test and Characterization Plan**

See individual proposals.

**Design for MOSIS Educational Program (Research)**  
**An improved 10GHz R<sup>2</sup>TWO distributed oscillator for low-power, low-skew, and low-jitter global clock generation/distribution**

**Prepared by:** Ruilin Wang (Grad Student) and Cheng-Kok Koh (Professor)

**Institution:** School of Electrical and Computer Engineering, Purdue University

**Date of Submission:** May. 8, 2007

**(Date of first Submission:** Apr. 13, 2007)

**(Date of first approval:** Apr. 17, 2007)

This proposal requests support for the fabrication of an improved 10GHz R<sup>2</sup>TWO distributed oscillator for low-power, low-skew and low-jitter global clock generation/distribution. The circuit has been designed by Ruilin Wang, a graduate student, for an unfunded research. An earlier design of R<sup>2</sup>TWO distributed oscillator by the same author was fabricated with a TSMC 0.18um Mixed-Signal CMOS process founded by MOSIS MEP. The functionality was verified and the measured performance metrics, i.e., skew, jitter, and power consumption, agreed with the theory. A paper based on this work was published in CICC2006 [7]. The main purpose of this project is to demonstrate the tunability of a new R<sup>2</sup>TWO oscillator that operates at a higher frequency (8-10GHz). This project will also demonstrate the scalability (for future technology) of the new distributed oscillator with improved skew, jitter, power consumption for future high performance processors under a more advanced CMOS process technology. IBM 8RF-DM 0.13um Mixed-mode or better is the target fabrication process.

**Proposed Design**

The details of the working mechanism of R<sup>2</sup>TWO are described in [7] (see attached). In the design presented in [7], the oscillation frequency is designed to be around 6.5GHz on purpose due to the bandwidth limitations of 0.18um CMOS technologies. The main shortcoming of that design is that although the oscillation frequency is high, it is fixed and determined by the circuit parameters. However, in order to deploy this R<sup>2</sup>TWO oscillator in the future multi-gigahertz clock distribution/generation network, the oscillation frequency should be tunable so that the clock frequency can be synchronized with an external crystal oscillator. Moreover, although R<sup>2</sup>TWO is theoretically scalable and should give lower skew and jitter with process scaling, there are no fabricated chips with more advanced technology (e.g., 0.13um CMOS or better with copper interconnect) to validate this claim.

In the proposed design, we use distributed varactors to control the oscillation frequency. The varactors are distributed along the transmission line with pull-up and pull-down pairs in order to guarantee the symmetry of the waveform. Based on the simulation results obtained with Agilent-ADS, the tuning range can be up to around 30% of the oscillation frequency and the phase noise can be lowered by around 5-10 db. Although the proposed design can easily oscillate at a frequency of 15GHz with 0.13um CMOS model, the designed oscillation frequency is 8 to 10GHz in order to accommodate the limitations of the available test equipments. The power saving with varactors and 0.13um technology is still more than 60% according to our simulation. To the best of our knowledge, the results are still better than other recently proposed schemes [1] [2] [3]. For ease of

measurement, a specially-designed on-chip skew detection circuit based on the Gilbert multiplier cell will also be included.

### **Fabrication Process**

IBM 8RF-DM 0.13um

### **Anticipated Design Size**

2mm × 2.5mm

### **Packaging Requirements**

The chip packaging is preferred.

### **Simulation and Verification Plan**

The chip is a full custom design for which schematics and layouts are going to be prepared using Cadence Virtuoso. Depending on the vendor design kit, DRC and LVS will be performed to verify consistency between the schematics and layout with Cadence tools or Mentor Graphics tools. We will use Fastcap and Fasthenry [5] [6] to extract the RLGC parameters of the transmission lines these parameters. Very conservative values will be chosen for simulations. Functionality of the schematic has been verified by Agilent-ADS and HSPICE simulations, with both RLGC distributed model and transmission line model used for the top-layer lossy transmission lines. The HSPICE models used are BSIM3 level 49 obtained from the MOSIS website. After the layout is done, we will also perform post-layout HSPICE simulation for functionality and performance verification.

### **Test Plan**

Testing of the proposed oscillator for global clock distribution will include functional verification, performance testing, and power consumption measurements. Equipments available for the testing include (but not limited to):

1. An Agilent 86100A digital oscilloscope with 20GHz sample rate input modules.
2. A Keithley 6430 Sub-Femtoamp SourceMeter for both static and dynamic power measurement.
3. A Tektronix 2755 spectrum analyzer and an Agilent E4448A spectrum analyzer.
4. A digital multi-meter.
5. A Tektronix probe station
6. A milling-machine for making PCB.

Test to be performed:

1. Skew measurement: Since the skew is in the order of picoseconds, it is very difficult to measure it from outside of the chip with the available equipment. To overcome that, we have designed an on-chip Gilbert analog multiplier to convert the phase difference (skew) of the clock signals at every two sinks into DC differential voltages, and will use multi-meters to test the voltages off chip. The skew values can be obtained with computations (conversions) from the voltage values. We will intentionally change the corner power supply voltage to see the influence on skew (three independent Vdd pads will be placed on

the chip). We will also vary the temperature distribution to see its influence on skew, if the test condition is available.

2. Jitter measurement: Since directly outputting the clock signals to the outside probe may change the working condition of the oscillator, we will use source-follower buffers to route the signals outside. We plan to use the available power spectrum analyzer to get the phase noise spectrum, which is a good indicator for the amount of RMS jitter. We also plan to inject power supply noise and test the noise spectrum thereafter if the test condition is available.
3. Power consumption measurement: The test circuitry will be turned off to obtain the correct supply current and hence the correct power consumption measurement. As a reference, the proposed R<sup>2</sup>TWO will also be operated as a traditional ring oscillator to measure its power consumption. The power saving can thus be obtained.
4. The sensitivity of frequency vs. power supply: From simulations, the clock period is insensitive to power supply voltage variations; the variations in clock period is around 0.3ps for a 10% variation in power supply, with the presence of varactors. In order to verify that the frequency is insensitive to power supply voltage variations, various power supply voltages (from -10% to +10% of the deviation from the power supply voltage) will be applied. And the frequencies, as well as the frequency variations, will be measured.

### **Reporting Plan**

Once the chip has been fabricated and tested, a report will be submitted to MOSIS that will include the following information:

1. Schematics, layout and a detailed explanation of the design.
2. HSPICE and Agilent-ADS simulation results for clock skews (between the three clock sinks) with proper assumptions of process variations, power supply variations and temperature variations.
3. HSPICE and Agilent-ADS simulation results for the power consumption.
4. HSPICE simulation results for clock jitters with power supply noise injected, and Agilent-ADS phase noise simulation results.
5. Results from each of the tests described in the test plan.
6. A comparison and analysis of differences between the simulation results and the test results.
7. Conclusions and recommendations regarding this improved oscillator for global clock distribution and the accuracy and relevance of simulated circuit performance.

### **Project Participants**

The chip was designed and will be tested by Ruilin Wang. Ruilin Wang is a Ph.D. candidate studying VLSI interconnect circuit design and automation in the School of Electrical and Computer Engineering at Purdue University. He received his B.S. and MSEE. degree in Microelectronics from Xi'an Jiaotong University in China.

The work of Mr. Wang is supervised by Prof. Cheng-Kok Koh of the School of Electrical and Computer Engineering at Purdue University. He obtained the Ph.D. degree from UCLA and has

been a faculty member at Purdue University since 1998. Prof. Koh supervises a research group specializing in high performance VLSI design and design automation of VLSI.

Assisting Mr. Wang with design flow issues and the MOSIS submission process is Dr. Mark C. Johnson. Dr. Johnson is a professional staff member in the School of Electrical and Computer Engineering at Purdue University. Dr. Johnson is a 1998 Ph.D. graduate of Purdue University in the area of design automation for high performance and low power VLSI. Dr. Johnson's official responsibilities are in the area of laboratory and curriculum development, but he is also active in research and consulting in the area of CAD for VLSI.

## References

- [1] F. O'Mahony, C. Yue, M. Horowitz and S. Wong. "A 10-GHz global clock distribution using coupled standing-wave oscillators". *IEEE Journal of Solid-State Circuits*, 38(11):1813–1820, Nov. 2003.
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- [4] Taiwan Semiconductor Manufacturing Co., LTD. "TSMC 0.18UM LOGIC 1P6M SALICIDE 1.8V/3.3V SPICE MODELS".
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- [6] M. Kamon, M. J. Tsuk and J. White, "FASTHENRY: A Multipole-Accelerated 3-D Inductance Extraction Program," *IEEE Trans. on Microwave Theory and Techniques*, September 1994, vol. 42, no.9, p. 1750-1758.
- [7] Ruilin Wang, Cheng-Kok Koh, Byunghoo Jung and William Chappell, "Clock Generation and Distribution using Traveling-wave oscillators with Reflection and Regeneration", Proceedings of the conference of custom integrated circuits, 2006, p.781-784.

**Design for MOSIS Educational Program (Research)**  
**Low Noise Amplifier and Power Amplifier**

**Prepared by:** Sanghoon Joo (Grad Student), Mac Inerowicz (Grad Student), Charles Chen (Grad Student) and Byunghoo Jung (Professor)

**Institution:** School of Electrical and Computer Engineering, Purdue University

**Date of Submission:** May. 8, 2007

We have been studying new RF circuit topologies that can provide ultra low-power and robust operation. Low noise amplifier (LNA), power amplifier (PA), and built-in self-test and calibration circuit in IBM 0.13um technology will be included in the submission.

**Project Description**

(1) 2.4GHz low noise amplifier (LNA) using passive amplification:

This design uses a new topology based on passive amplification and resistive feedback for impedance matching and low-noise. The design targets 2.4GHz narrowband operation. This topology can be used for any narrowband wireless communication system. We plan to apply this technique for wideband LNA design in the future.

(2) Power amplifier (PA) with integrated differential to single-ended converter:

This design uses a new topology that can convert differential input signal to single-ended output signal without using external balun. This compact design can provide low-cost solution for PA design for short distance applications.

(3) Built-in self test and calibration circuit:

A built-in current sensor that does not degrade the performance of the device under test has been developed. The built-in current sensor, calibration circuit, high-gain amplifier, and benchmark device are included. This sensor can be used for on-line testing for RF circuits and microprocessors.

We believe the RF circuits described above can lead to solutions for ultra low-power and robust radio systems. These ultra low power radio systems will find useful applications such as sensor network and bio-telemetry. This project is not funded. We will be seeking for fund opportunities for the research on integrated ultra low-power radio design and applications, and the fabrication support from MOSIS for this project will be very helpful for our future endeavor.

**Fabrication Process**

IBM 0.13um CMOS

**Anticipated Design Size**

2mm × 2mm

**Packaging Requirements:**

No package is required.

**Simulation Plans**

Cadence Spectre simulation performed for each design is summarized below;

- LNA: S-parameters, noise figure, power consumption, and linearity (IIP3 and IdB compression point)
- PA: Gain, matching, power efficiency, and linearity
- Built-in self test: Gain, linearity, and noise figure with and without auto-calibration

**Test and Characterization Plan**

- LNA: S-parameter, noise figure, power consumption, IIP3, and 1dB compression point will be measure using network analyzer, noise figure meter, and spectrum analyzer, respectively.
- PA: Gain, matching, and power efficiency will be measure using network analyzer and power meter, respectively.
- Built-in self test: Gain and linearity will be measured using network analyzer, and spectrum analyzer. The internal control signal will be measure using oscilloscope to monitor automatic calibration.

**Design for MOSIS Educational Program (Research)**  
**Phase Locked Loop and SRAM**

**Prepared by:** Jaydeep K. Kulkarni (Grad Student), Sang Phill Park (Grad Student), and  
Kaushik Roy (Professor)

**Institution:** School of Electrical and Computer Engineering, Purdue University

**Date of Submission:** May. 8, 2007

**Project Description**

**1. Phase Locked Loop:**

Our test chip is targeted to demonstrate a variation resilient circuit design methodology under process variation and reliability degradation. Through a set of analysis, we have shown that phase locked loop (PLL) circuit can function as an efficient and accurate dynamic sensor to capture on-chip process skew.

**2. SRAM:**

We will also implement a novel SRAM bitcell. Two memory arrays containing the 6T cell and proposed bitcell will be characterized. In addition, we will be implementing bitline sensing technique for SRAMs. The conventional technique and the proposed technique would be compared for different scenarios.

**Fabrication Process**

8RF-DM 0.13 $\mu$ m (29<sup>th</sup> May)

**Packaging Requirements**

All test chips needs to be packaged. No bare die requirement.

**Estimated Design Size**

Each design is 2mm X 1mm; total 2mm X 2mm

Pins required in total = 100

**Simulation Plans**

The designs will be verified with rigorous HSPICE Monte Carlo simulations.

**Test Plans**

**1. PLL:**

We will test the accuracy and sensitivity of our sensor circuit under various operating conditions by altering 1) temperature, 2) power supply (VDD), and 3) process corners. Furthermore, our sensor circuits will be combined to a general purpose ALU circuits to implement a variation resilient circuit system. In this system, first, an optimal adaptive body bias (ABB) is computed by using our sensor circuit. Then, by applying ABB, it will be shown that even under a severe process skew, target circuit (ALU) will properly operate without occurring any functional or parametric failures.

**2. SRAM:**

Isolated memory structures with appropriate guard rings and dummy devices would be used to measure static noise margins. SRAM tester circuits would be implemented in order to estimate the memory failure statistics for various supply voltages.

**Design for MOSIS Educational Program (Research)**  
**A Programmable RF Matching Network**

**Prepared by:** Hanil Lee (Grad Student), and Saeed Mohammadi (Professor)

**Institution:** School of Electrical and Computer Engineering, Purdue University

**Date of Submission:** May. 8, 2007

**Project Description**

In this project we use a combination of shielded transmission lines loaded periodically with PMOS varactors to achieve a fully reconfigurable matching network. Shielded transmission lines on Si substrate have been recently demonstrated. Their loss performance is significantly improved compared to standard transmission lines as they do not suffer from dielectric losses that are dominant at higher frequencies. This has resulted in improving the loss of transmission lines by almost 2dB/mm at 10GHz compared to standard implementation. We will take advantage of these low loss transmission lines to design a reconfigurable matching network based on a double-slug tuner architecture. The transmission line is periodically loaded with varactors. Each varactor is connected to a shift register data line that contains information whether the varactors should be in high capacitance or low capacitance mode. The capacitance variation achieved by varactors can load the transmission line resulting in a change in the impedance of the line. By changing the data in the shift register through a serial link, one can decide the length of different sections on transmission lines that have different characteristic impedances. Therefore the impedance seen from the port can be adjusted by varying the length of these sections.

**Fabrication Process and Packaging requirement**

We plan to use IBM 8RF technology for the first demonstration. We do not require any packaging as the chip will be characterized using on wafer probing techniques.

**Estimated project Size**

An estimated size of 2mmx1.5mm is required. This is necessary for test structures as well as the tunable matching network.

**Simulation Plans**

We will use a combination of Cadence Specter RF and Ansoft HFSS as well as Agilent ADS for the design of the reconfigurable matching network. Cadence is used to perform circuit simulation and layout design. Agilent ADS is used to perform system simulation to indicate which areas on the Smith Chart will be covered. An optimization in ADS is necessary to cover as much of the Smith Chart as possible. Finally HFSS is used to simulate the shielded transmission lines loaded with varactors.

**Test and Characterization Plans**

Testing will be performed at Birck Nanotechnology center using on-wafer probing and an Agilent 8510XF network analyzer. We expect the circuit to perform from frequencies above 10GHz and possibly up to 40GHz.