Design for MOSIS Educational Program (Research)

Project Title:
Modeling the Substrate Noise Coupling on PMOS and NMOS Mixers

Prepared by: Chikuang Yu, and Prof. Kenneth K. O

Institution: Electrical and Computer Engineering/ University of Florida

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Modeling the Substrate Noise Coupling on PMOS and NMOS Mixers (A Research Proposal for MEP)

Prof. Kenneth K. O, University of Florida
Silicon Microwave Integrated Circuit and System Research Group(SiMICS)
Department of Electrical and Computer Engineering, University of Florida,
538 Engineering Blg., Gainesville, FL 32611;Tel. (352)392-6618;e-mail:kko@tec.ufl.edu

Overview

Mixers are one of the critical building blocks in modern communication systems. They downconvert the receiving RF signal to lower intermediate frequency (IF frequency) or directly to DC in a receiver chain, which allows the signal easily amplified and the noise simply suppressed. They also upconvert the signal at IF frequency to higher frequency in a transmitter chain so that the signal can easily be broadcasted through the air. However, they are vulnerable to the substrate noise. As the CMOS technology is scaled, more high frequency CMOS analog circuits, mixed-signal circuits, and digital circuits can be integrated on a single chip. A serious concern for such a system is the noise coupling effect. The noise from digital circuits can couple through the substrate [1] and, then, generate unwanted spurs and noise in interested band of the mixer. These spurs and noise can severely degrade the mixer performance. These processes include the direct coupling and the indirect intermodulation with the desired RF signal.

In order to understand the fundamental mechanism of these processes, the substrate resistance test structure will be built in this project to measure the substrate resistor network between the digital circuits and mixer blocks, shown in Fig. 1. All these test structures will include two parts: the tapered buffers which represent the digital circuits and the mixers. Additionally, the PMOS mixer test structures will be built using the same method to compare the noise coupling with that for the NMOS counterparts.

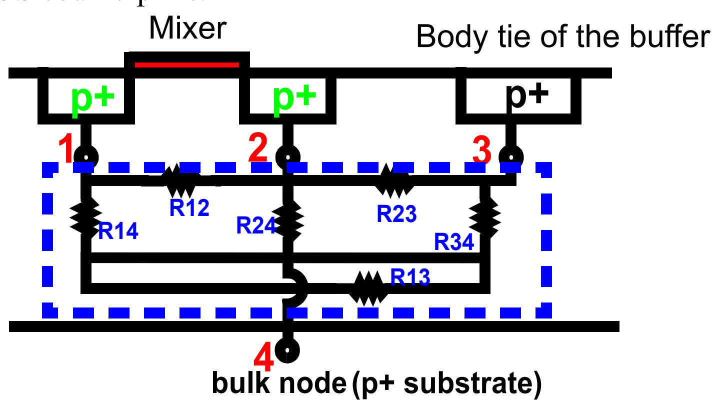

Fig. 1 substrate resistance model

Project Description

The mixers are Gilbert cell double balanced active type as shown in Fig. 2. Intermediate frequency (IF) is chosen to be 20 MHz and RF is 2.4 GHz. Both mixers have an identical structure except for the fact that all the NMOS transistor are replaced by PMOS transistors. The tapered buffer is 8-stage and has a 2pF capacitive load in order to produce sufficient noise for observation.

All the circuits will be packaged and measured on a PC board. Because both mixers and buffers are electrically grounded through several down-bonds as shown in Fig. 2, this increases the noise

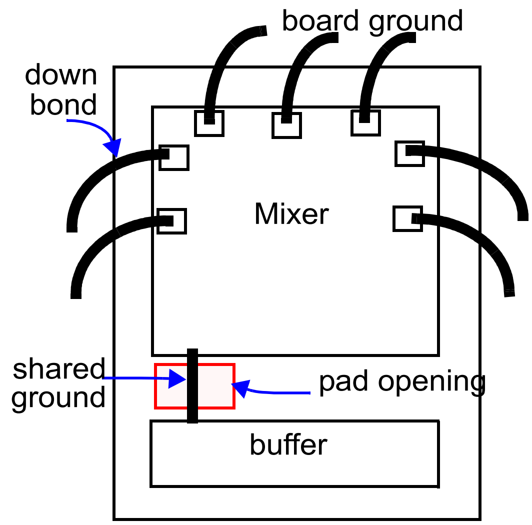

Fig. 2 the conceptual chip diagram

coupling possibility to mixer circuits. Evaluating the effect of this down-bond inductance to the coupling is import and critical. In addition, the effects of the on-chip-ground connection between the mixer and the buffer will be investigated.

In these circuits, all noise-sensitive-nodes such as drain/source of transistors, input/output pads, n-wells and PGS (poly ground shield) will be replaced by p+ or n+ diffusion areas. These areas are noted as substrate ports and represent the nodes in the substrate resistor network. By

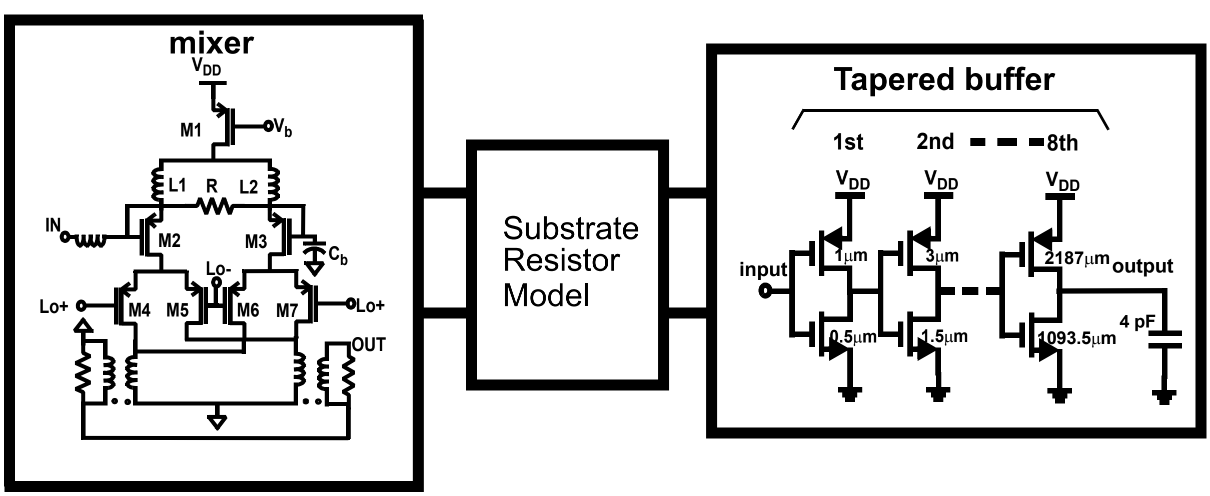

Fig. 3 Circuit level simulations

measuring the resistance between any two of these nodes, the substrate network model will be constructed and this measured model will be compared with the SubstrateStorm (a substrate noise simulation tool) simulation result to further understand the fundamental noise coupling mechanism through the substrate. Also, this model will be combined with the original circuits to simulate the substrate effect and to understand the coupling path between the tapered buffer and the mixer as shown in Fig. 3.

Fabrication process

For this project, we plan to use the TSMC 0.18µm technology scheduled on Jan. 10, 2005.

Packaging requirements.

No packaging is required for this project.

Estimated Project Size

The layout includes PMOS/NMOS structures (3 mm^2), noise generation circuits (3 mm^2), and associated DC/AC test structures (2.816 mm^2). So the total area is "**2.13 mm x 3.2 mm**".

Simulation Plans

We are using SpectreRF to simulate and optimize all circuits, Cadence Virtuoso to do the layout, and Fast Harry and Matlab to design the passive components. To minimize the process variations and errors, SubstrateStrom is used to identify the most impacted area in the circuits and refine the test structure design.

Test and Characterization Plans

The measurements will be made not only on chip but also in a package. The chips will be packaged in an SOIC-like package and characterized. The HP4155 DC measurement setup will be used to measure the resistance network. An example for two-port measurement of a resistive network is shown in Fig. 4.

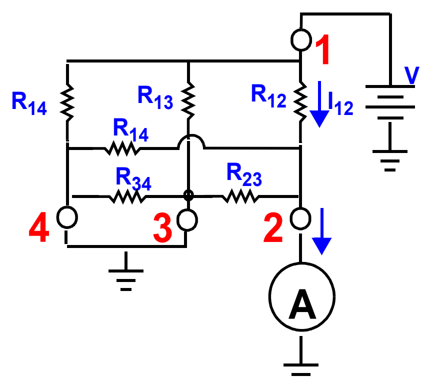

Fig. 4 DC measurement setup

References

[1] R. Rosst et al., "Model and Verification of Triple-Well Shielding on substrate Noise in mixed-Signal CMOS IC's," *Proc. ESSCIRC*, pp. 643-646, Sep. 2003.