Report for MEP research fabrication

To: MOSIS
From: Dr. Randall Geiger, Iowa State University

Design: 62237
Fab ID: T13V-AC
Design Name: High gain Opamp
Technology: SCN3ME_SUBM (AMI C5N)
Designer: Jie Yan

Original Proposal:

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Title: Building Blocks for High Gain Fast-settling Amplifier Circuits

I would like to request fabrication support for a project focusing on the design of robust high gain fast-settling CMOS amplifier circuits. The project concentrates on the design of very high DC gain and fast-settling amplifiers with negative impedance compensation technique in standard CMOS processes. Such amplifiers are the key components to build high speed Analog-to-Digital converters (ADCs).

Op amps play an important role in many analog and mixed-signal systems. As device feature sizes have been reduced, the realization of high-gain amplifiers with large Gain-Bandwidth-Products (GBW) in processes with decreasing supply voltages has become challenging. As the supply voltage is reduced, a key limitation that arises is a significant reduction in the number of devices that can be stacked between the power supply rails. Traditional gain enhancement techniques exploiting cascoding are becoming unviable. This project proposes a new circuit technique for voltage gain enhancement in CMOS Op Amp design suitable for low voltage and high speed operation. A negative conductance is used to cancel the positive output conductance of an amplifier thereby reducing the total equivalent output conductance and increasing the voltage gain of the amplifier. The negative conductance is derived from the output conductance of a transistor, as opposed to a transconductance or some other parameters, to enhance tracking over process and environment variations. The negative impedance compensation approach offers potential for the most gain enhancement with low power dissipation, low voltage operation and excellent high frequency performance. In this project, we exploit the negative impedance gain enhancement technique with an approach that significantly reduces the gain variability to the compensating impedance.

A fully differential CMOS op amp using proposed negative conductance gain enhancement technique is designed. Simulations show that for AMI 0.5um CMOS technology with a power supply of 3V, a dc gain of more than 94dB is achievable with the proposed amplifiers. Settling measurements with a feedback factor of $\beta = ½$ show fast settling behavior and a settling accuracy of better than 0.1% for a 1.2V input step.

We are requesting support for fabrication of this circuit under the RESEARCH program that was initially announced by MOSIS. We have the designs nearly completed in the AMI 0.5u CMOS process and would like to fabricate the circuit in this process in the March run. The circuit has been simulated using HSPICE over process corners using

BSIM 3 models under the CADENCE framework we have available on the ISU campus. The circuit will be tested in the Carver Laboratory, facilities that are currently available on the ISU campus. The University has made an investment of between $1million and $1.5million for the equipment in these laboratories much of it coming in the past 2 years. The total silicon area needed for this project is estimated at 2.25mm^2. We also request packaging and prefer to a combination of packaged and unpackaged parts.

Project Request Summary:

Program:	RESEARCH
Process:	AMI 0.5u
Estimated Die Area:	2.25mm^2
Process Run:	March 26, 2001
Packaging:	DIP40

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Test Report for High Gain Fast-settling Amplifier Circuits

The project concentrates on the design of very high DC gain and fast-settling amplifiers with new negative impedance compensation technique in standard CMOS processes.

A prototype two-stage fully differential high gain amplifier was designed based on the proposed negative conductance gain enhancement technique to validate the fundamental performance characteristics of the negative conductance gain enhancement technique. The amplifier was fabricated using the AMI Semiconductor (AMIS) 0.5um SCN05 process through MOSIS in run T13V.

The amplifier was tested with ±1.5 V supply voltages. The negative conductance is adjustable by changing the control voltage Vctl. Therefore, the DC gain is adjustable with the control voltage. Fig. 1 shows the measured differential open-loop DC gain versus the control voltage Vctrl. An open-loop DC gain of 83dB was measured for a control voltage Vctrl of -0.74507 Volts.

By keeping the control voltage fixed, the relationship between the DC gain and the output differential voltage Vod was measured. This is shown in Fig. 2.

In summery, a fully differential CMOS operational amplifier using a new negative conductance gain enhancement technique was designed. The amplifier was realized in an AMI 0.5 um CMOS process and had a measured DC gain of 83dB. With a 3 Volts supply, power consumption is 45mW. The gain is over 60 dB for a 240mV output range. Test results validated the fundamental performance characteristics of the proposed negative conductance gain enhancement technique.

NOTE: Two papers have been published for this project:

1. J. Yan and R. L. Geiger, "A High Gain CMOS Operational Amplifier With Negative Conductance Gain Enhancement," IEEE Custom Integrated Circuits Conference, May 2002 .

2. J. Yan and Randall Geiger, "Fast-Settling CMOS Operational Amplifiers with Negative Conductance Voltage Gain Enhancement", Proceedings of 2001 IEEE International Symposium on Circuits and Systems, pp 228-231, Sydney, May 2001

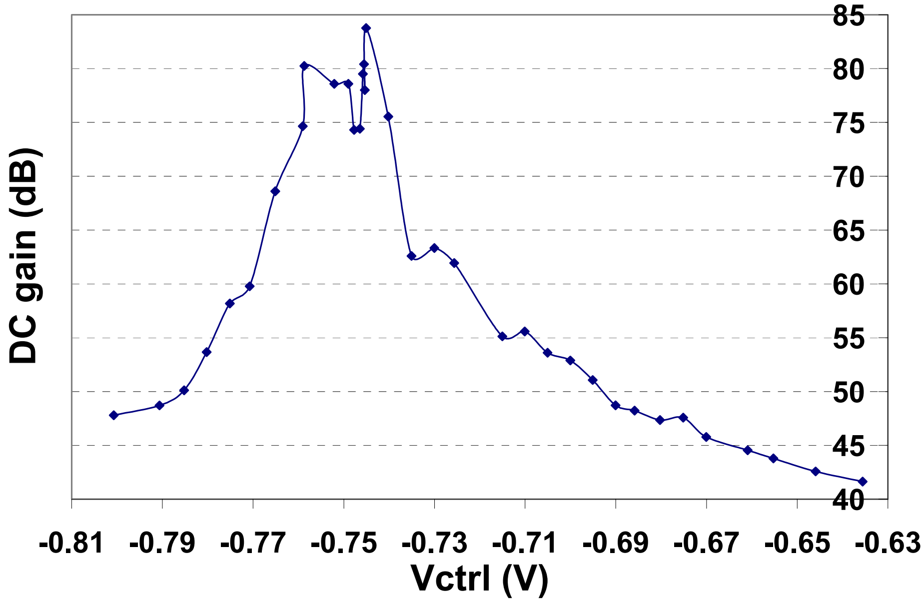

Fig. 1 Measured DC gain versus the control voltage Vctrl

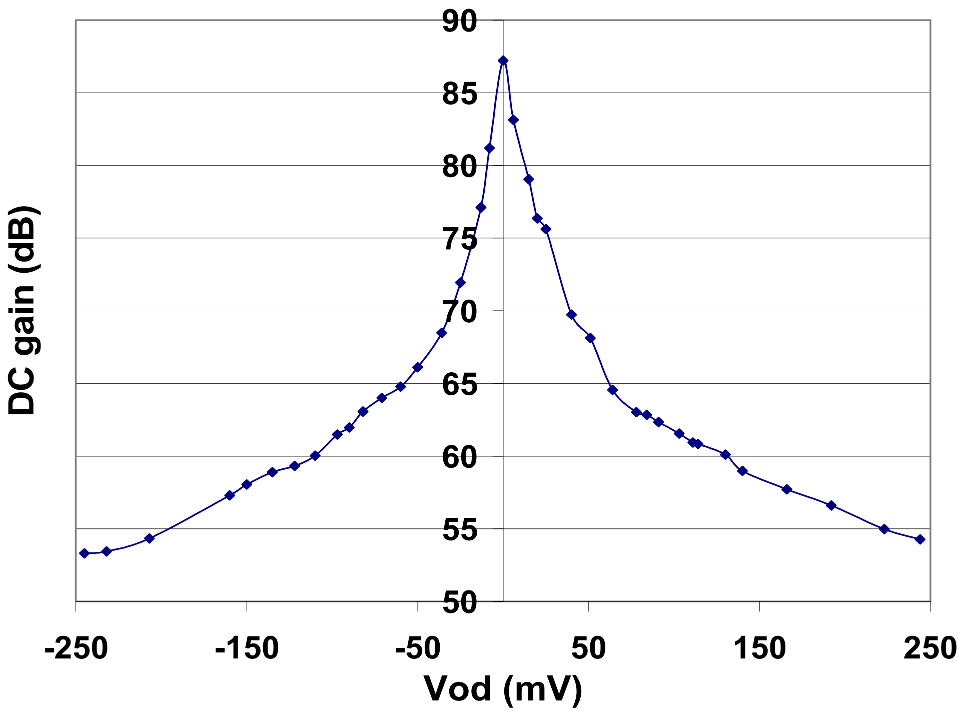

Fig. 2 Measured DC gain versus the differential output voltage Vod