Request for MOSIS support under the Research Program for silicon fabrication

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Title: Building Blocks for High-Frequency Communication Circuits

Project Description:

I would like to request fabrication support for a project focusing on the design of robust high-frequency communication circuits. The project concentrates on the building blocks needed to build high frequency transceivers that support multi G-bit serial data transmission rates in standard CMOS processes. To that end, we are currently working on three blocks that are needed in such systems.

One is a VCO architecture that offers process and temperature compensation. With this approach, the process and temperature compensated VCO can be designed with an oscillation frequency sensitivity to the loop filter output that is reduced dramatically from what is inherent in existing VCO architectures. In the circuit we have been working on, simulations suggest a reduction in the sensitivity by more than a factor of 10 over what is attainable without the compensation. This results in a corresponding drop in the jitter of PLLs that utilize the YCO. A prototype VCO designed to operate at a nominal oscillation frequency of 2 GHz over process and temperature has been designed in the 0.25u TSMC CMOS process.

The second focuses on building very high frequency CMOS filters that can be used as channel equalizers. In several widely used existing high-speed serial communication standards, a modest-performance adaptive equalizer on the front end of the receiver can substantially reduce the inter-symbol interference and correspondingly the bit error rate (BER). Although these adaptive filters do not need high order or precise pole positioning and do not require a large spurious free dynamic range (SFDR), they do require very high frequency poles with pole positions that must be in the several G-Hz frequency range for some of the higher-speed standards. We have been working on a new class of filters termed "VCO-derived filters" that operate with pole frequencies comparable to the nominal oscillating frequency of the parent VCO. The strategy in using these VCO-derived structures is to take advantage of the design efforts that have gone into building high speed VCOs and to essentially re-use the delay stages of the VCO in an adaptive filter. The pole frequencies we can achieve in these filters are up to about 6 GHz in a 0.25u CMOS process. Prototype low-pass and band-pass filter designed in the TSMC 0.25um process have been designed. Simulation results for the low-pass filter designed for a cutoff frequency of 6 GHz show a THD of -40 dB for a 400mV peak-peak sinusoidal input. The band-pass filter has a resonant frequency programmable from 4 GHz to 5.18 GHz, a programmable Q from 4 to 89 and mid-band THE) of -40 dB for a 200mV peak-peak sinusoidal input signal.

The third project focuses on the design of a very high frequency phase detector. In high-frequency clock and data recovery applications, the clock is generally derived from a PLL that is comprised of four fundamental blocks, a VCO, a phase detector, a charge pump, and a loop filter. The major bottleneck in extending the frequency of operation of these PLLs is the phase detector. Although building a phase detector that can lock onto a clock signal is reasonably straightforward, phase detectors that accurately detect phase in a data sequence that has varying numbers of consecutive ones and zeros is somewhat more challenging. The two most popular phase detectors for these applications are the Hogge phase detector and the Alexander phase detector both of which use flip-flops to avoid loss of phase information in the absence of data transitions. Correspondingly, the speed of operation of these phase detectors is limited with the delays in the sequential logic circuits (flip-flops). We have designed a new phase detector that is based on simple combinational logic circuits that operates at substantially higher data rates than is achievable with the Hogge and Alexander phase detectors in comparable processes. Simulations suggest approximately a factor of 2 improvement in speed is achievable with the new structure. In contrast to existing phase detectors which accept inputs only from the data and VCO output, the new phase detector uses phase-lead and phase-lag signals from the VCO to circumvent the need for sequential logic circuits.

We are requesting support for fabrication of these three circuits under the RESEARCH program that was initially announced by MOSIS. We have the designs nearly completed in the TSMC 0.25u CMOS process and would like to fabricate these circuits in this process in the December run.

Estimated Project Size: 7mm^2 in TSMC 0.25u CMOS process
We prefer to work with unpackaged die so that we can manage the parasitic capacitances inherent at the speeds we are working.

Simulation Plans
The circuits have been simulated using HSPICE over temperature and process corners using BSIM 3, level 49 models under the CADENCE framework we have available on the ISU campus.

Test and Characterization Plans
The circuits will be tested in the Carver Laboratory and the RF Circuits laboratory, facilities that are currently available on the ISU campus. The University has made an investment of between $1 million and $1 .5million for the equipment in these laboratories much of it coming in the past 2 years.

Note:
This project was fabricated before in March TSMC 0.25u run. The test results show that the pad is open. The padframe was designed in SCMOS technology code while our design was based on vendor rule. When the padframe was streamed in, the contact size was not correctly scaled which leads to open-circuit of the pad.