MOSIS MEP RESEARCH PROPOSAL

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October 2001

The proposed chip is intended to demonstrate a design for test (DFT) scheme for practical communication circuits.

1. Project Description:

We would like to submit a communications IC chip, to be implemented on the TSMC 0.35um, through MOSIS's MEP RESEARCH program.

The chip will mainly serve to prove a mixed-signal Built-In Self-Test (BIST) concept, developed at the Santa Clara University as a Ph.D research program. The concept has applications in testing the functionality of high-speed transmitters and receivers (transceivers) on a modern data communications chip. Under the research program, practical circuits have been developed to apply the concept on an IEEE 1394a data communications system.

A general block diagram of a data communications chip is shown in Fig. 1. Depending on the level of integration, the Link may or may not be on the same chip. The Physical Signaling block communicates with the Link, and on the Transmit side, a Transmitter (TX) takes data from the Physical Signaling block; encodes the data per communications standards; and outputs to the outside world. On the Receive side, a receiver (RX) takes data from the outside world; appropriately decodes that before sending it back to the Physical Signaling block. As depicted in the figure, the current trend is to have more than one pair of TX and RX blocks or ports. The BIST structure proposed here utilizes this trend to do functional testing of various sub-blocks in the TX and RX.

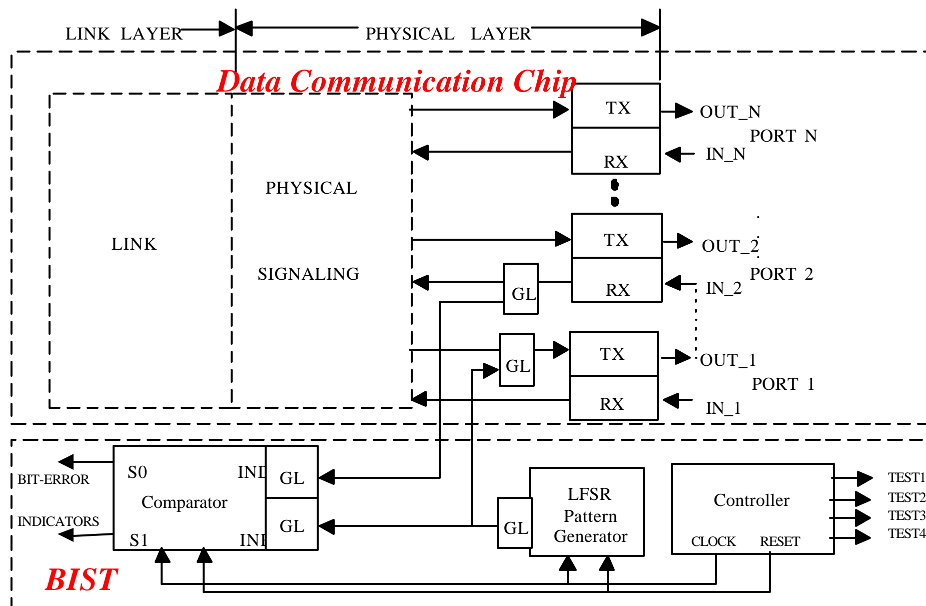

Figure 1

The proposed 0.35um silicon implementation consists of 3-port IEEE 1394a Physical Layer device, capable of handling 400Mbps data rates. The chip also consists of mixed-signal Built-In Self-Test (BIST) structures to do self-testing of the high-speed data transmitter and receiver blocks.

2. Advantages of BIST:

A short description on advantages offered by BIST techniques is in order. In a customary ATE testing of an integrated-circuit chip, the device under test (DUT) is seated at a test head, and long cables are used to connect the test head and the processing boards of the tester. The test head accesses the pins of the DUT through circuitry called 'pin electronics'. Because of the complexity involved in the whole test set up, along with capacitive and inductive loadings introduced by the cables and pin electronics, at-speed testing of modern high-speed chips is expensive, time-wise and money-wise.

Built-In Self-Testing (BIST) techniques perform on-chip self-testing of the chip (or part of the chip). The motivation in BIST techniques lie not only on the fact that they can reduce the number of tests to be performed by the ATE during manufacturing, but also on the fact that they can perform tests in the field. Also the capacitive and inductive loadings to the circuits under test (CUT) by the BIST circuitry are well controlled as they sit right on the same chip. That makes the at-speed testing easier and more reliable.

3. Estimated Project Size:

The chip, including the BIST structure occupies about 4000um X 5000um in 0.35um design rules.

4. Simulation Plans:

The proposed circuit being a mixed-signal IC chip, we plan to do analog transistor-level simulations. Due to the complexity, simulations will be done in 3 phases, namely: Cell-level, Block-level, and Chip-level simulations.

Some examples of the Cell-level circuits are charge-pumps, comparators, etc. In this level, simulations will be done using HSPICE (Avanti) software.

Cell-level circuits are connected together to form Block-level circuits. Some examples of the Block-level circuits are Phase-locked loops and speed-detection blocks. In this level, simulations will be done using HSPICE and HSIM (Nassda) software.

Block-level circuits are, in turn, connected together to form the Chip. In the Chip-level, simulations will be done using HSIM.

5. Test and Characterization Plans:

Figure 2 shows the planned characterization set-up.

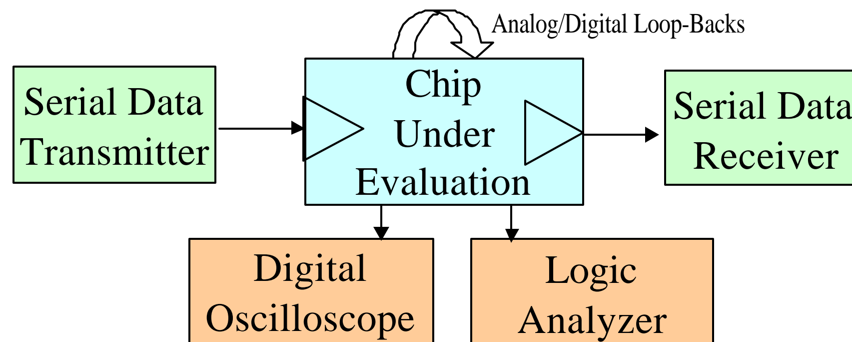

Figure 2

Equipment:

Serial Data Transmitter:	GigaBert-660 TX (Tektronix)
Serial Data Receiver:	GigaBert-660 DRX (Tektronix)
Digital Oscilloscope:	LeCroy 9374M (LeCroy)
	TDS694C (Tektronix)

In this set-up, the Serial Data Transmitter originating data, send the data through the 3-port IEEE 1394a Physical Layer device, and the output from the device analyzed by the Serial Data Receiver. The Oscilloscopes and Logic Analyzers are used to capture the analog and digital data. In the BIST mode, the additional test pins of CUT indicate the pass or fail of self-test results.

Characterization Plan:

Characterization Plan for BIST Enhanced 3-Port IEEE 1394A

Item	Test Item		Completion Date	Days
		packaged chip back:	7-Jan-02	
1	**Functional Test**			
1-1	Transmit function test		10-Jan-02	3
1-2	Receive function test		14-Jan-02	2
1-3	BIST function test		16-Jan-02	2
2	**Electrical Characteristics Test**			
2-1	Transmit electrical test			
2-1-1	S400 Transmit Rise/Fall Timing Test		17-Jan-02	1
2-1-2	S200 Transmit Rise/Fall Timing Test		18-Jan-02	1
2-1-3	S100 Transmit Rise/Fall Timing Test		21-Jan-02	1
2-2	BIST test			
2-2-1	Bit Error BIST		4-Feb-02	10
2-2-2	Rise/Fall BIST		18-Feb-02	10
2-3	DC biasing test		19-Feb-02	1
2-4	Clock test		21-Feb-02	2
		Total:		30

Reference:

S. Lin, S. Mourad and S. Krishna, “BIST at speed testing for data communications transceivers” Asian Test Symposium, pp. 216-221, Taipei, Taiwan, Dec. 2000.