

Research Proposal for IBM 6HP (0.25 micron, BICMOS) Process

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We were allocated 3 chips for the 5HP process from an earlier submission. The 5 HP process got pushed ahead and the student could not meet the deadline. We designed our circuit with 6HP to meet the deadline for the March submission. However, we did not realize that approval for 5HP restricted us to 5HP only. We are resubmitting part of the earlier this proposal for 6HP runs. The student has completed the design of the high gain high bandwidth instrument amplifier for ultrasonic detectors in 6HP. For this proposal we are requesting 1 chip for 6 HP run. We will complete the remaining 2 projects from our earlier proposal with the 5HP.

Professor Dhali took the IBM Si-Ge design course in Jan. 2002. He is familiar with the CAD and simulation tools and design issues related to the 6HP Si-Ge process.

The VLSI chips to be designed is a part of the project described below. The initial projects were done with discrete circuits. However most of these circuits lend to VLSI implementation, which would improve the performance. The basis of the circuits will be a folded cascode operational amplifier. Bipolar transistors will greatly aid in the design of amplifiers and filters.

Project Description:

Tuned instrument amplifier for ultra sound positioning system:

Ultrasound positioning systems require the measurements of time difference between reference signal and the echo signal. The system requires high impedance difference amplifiers tuned at 75 kHz. The structure of the instrument amplifier will be cascade of difference amplifier with feedback back path consisting of tuned circuit at 75 kHz.

High gain amplifiers and driving circuits are need to synchronously detect the ultrasound signal to maximize signal to noise ratio.

Estimated Project Size

The project will use several op-amps and drivers. We expect the project to take up the entire chip area (1.9mmx1.9mm).

Simulation Plans

Design of the IBM 5HP process will take place using Cadence Design Tools v. 4.4.6. Layout's are made using Cadence Virtuoso Layout Editor. Our simulator is Analog Circuit Design Environment, which incorporates specter. This simulator allows for transient, dc, ac, frequency response, and noise simulations. Since most of the designs will be for tunable amplifiers and filter, the frequency response tool will be of great use.

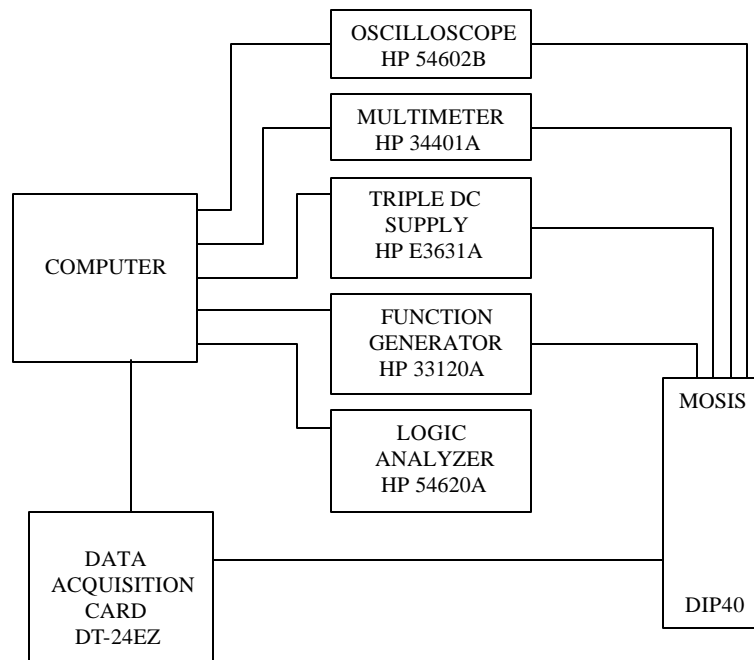


Fig1. Schematic of the testing facility

Test and Characterization plan

Testing the chip can easily be accomplished with the help of our Hewlett-Packard “HP-VEE” software and our HP hardware. The software is a visual programming language that produces shorter test development times. HP-VEE can be operated in either the visual language or a textual language, such as C or Visual Basic. The objects in this program perform functions such as I/O operations, analysis, and display. The user can easily accomplish analog input (A/D), analog output (D/A), digital input (DIN), digital output (DOUT), and counter/timer (C/T) operations. These operations are accessed through the use of a data acquisition card. This card can input either single-ended or differential input signals. The single-ended mode allows the user to input up to 16 channels, where as in the differential mode, 8 channels can be inputted. In addition to the two types of inputs, the data acquisition card provides two output channels as well. These outputs can be very useful in generating a multitude of analog and digital signals. The HP hardware includes an oscilloscope, digital multimeter, function generator, triple DC power supply, and a logic analyzer. A simple block diagram (Fig. 1) shows how all of these components and the data acquisition card are interfaced together.

Since all chips are a part of larger system, the final testing will be done on each system.