Phase Noise in Oscillators: A Research Proposal for the MEP

Shaun Johnson, Student, Stanford University   Tom Lee, Professor, Stanford University

***Abstract*-Further validation of the time-varying model of Phase Noise in Oscillators is needed. In addition, noise contribution due to the tail-current source in negative-resistance oscillator topologies is to be determined. Using the MOSIS .35um TSMC technology, we plan to design, simulate, and thoroughly characterize three 2.4GHz oscillators. Simulation will be done with SpectreRF while characterization will include using an RDL NTS-1000A phase noise measurement system, an HP 8563E Spectrum Analyzer and an HP 5500 phase noise measurement system. Jitter measurements may also be performed using a Tektronix CSA 803A signal analyzer.**

Overview

The continued betterment of phase noise in oscillators is required for the efficient use of our spectrum. Lower phase noise in oscillators translates into an increase in user capacity, something that service providers pay billions of dollars for. Research has shown that phase noise can be treated in a Linear, Time-Variant (LTV) fashion, yielding excellent results [1]. The purpose of this individually directed study is to further validate the predictions of this theory and understand the impact of the tail-current source on the total oscillator phase noise.

Project Description

To further validate the LTV theory presented in [1], we will build three oscillator structures. The first structure will be a 2.4GHz Colpitts oscillator (see Figure 1). The Colpitts has a reputation of being an excellent oscillator, but many people can't quantify why that is. We hope to put the spotlight back on the Colpitts and highlight the characteristics that make it such a great topology. In doing so, we will exploit the insights provided to us by the LTV theory.

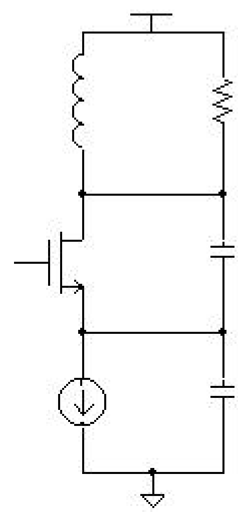

Figure 1: Colpitts Oscillator

In addition to achieving the typical Colpitts performance, we will filter out the 1/f noise of the current source to see if we can improve on this already remarkable topology.

In order to determine the noise contribution due to the tail current source in a VCO, the second and third oscillators will include two identical LC oscillators (see Figure 2). One oscillator will include a low-pass filter to attenuate the 1/f noise due to the tail-current source. The other VCO will remain unchanged. In this manner, we will be able to determine the impact of the filter (that is, the total up-conversion of the1/f noise of the tail current source) on overall noise performance of the oscillator. This data will be useful in the design of future oscillators.

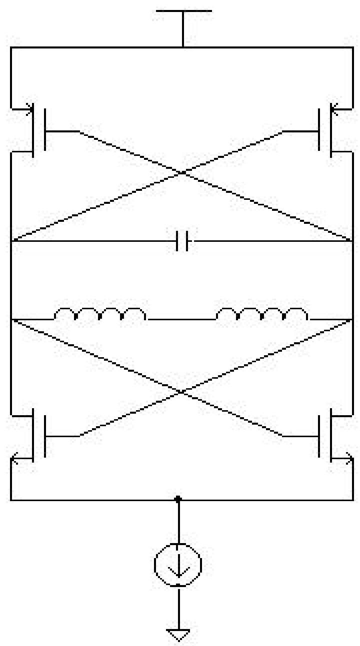

Figure 2: LC Oscillator

Estimated Project Size

The necessity of on-chip spiral inductors inherently requires an area hit. Taking capacitor/inductor area into account, we estimate the size of this chip will be approximately 2mm x 2mm.

Simulation Plans

We plan to simulate all oscillators with SpectreRF to find out the Impulse Sensitivity Function (ISF). In doing this, we will be able to calculate the noise-contribution due to various sources in our circuit and calculate what the phase noise performance of the overall system should be.

Test and Characterization Plans

To characterize our chip, we will be using an RDL NTS-1000A phase noise measurement system, an HP 8563E Spectrum Analyzer and an HP 5500 phase noise measurement system. Jitter measurements may also be performed using a Tektronix CSA 803A signal analyzer. We also intend to publish our results in the IEEE Journal for Solid-State Circuits.

Thomas H. Lee Bio

Thomas H. Lee received the S.B., S.M. and Sc.D. degrees in electrical engineering, all from the Massachusetts Institute of Technology in 1983, 1985, and 1990, respectively.

He joined Analog Devices in 1990 where he was primarily engaged in the design of high-speed clock recovery devices. In 1992, he joined Rambus Inc. in Mountain View, CA where he developed high-speed analog circuitry for 500 megabyte/s CMOS DRAMs.

He has also contributed to the development of PLLs in the StrongARM, Alpha and K6/K7 microprocessors. Since 1994, he has been a Professor of Electrical Engineering at Stanford University where his research focus has been on gigahertz-speed wireline and wireless integrated circuits built in conventional silicon technologies, particularly CMOS.

He has twice received the "Best Paper" award at the International Solid-State Circuits Conference, was co-author of a "Best Student Paper" at ISSCC, was awarded the Best Paper prize at CICC, and recently won a Packard Foundation Fellowship.

He is a Distinguished Lecturer of the IEEE Solid-State Circuits Society, and also of the Microwave Society. He holds thirteen U.S. patents and is the author of a textbook, "The Design of CMOS Radio-Frequency Integrated Circuits," Cambridge Press, 1998, and is a co-author of two additional books on RF circuit design. He is also a cofounder of Matrix Semiconductor.

References

[1] A. Hajimiri and T. H. Lee, “A general theory of phase-noise in electrical oscillators,” IEEE J. Solid-State Circuits, vol. 33, pp. 179-194, Feb 1998.