

# Broadband Continuous-Time Sigma-Delta Analog-to-Digital Conversion Using MOSIS AMI 0.5 $\mu$ m CMOS Technology

*A Research/Educational Proposal*

Shouli Yan and Edgar Sanchez-Sinencio

**Department of Electrical Engineering  
Analog and Mixed-Signal Center  
Texas A&M University,  
College Station, TX 77843**

June 29, 2001

## Rationale and Goals

In the past two decades, sigma-delta ( $\Sigma\Delta$ ) analog-to-digital converters are well suited for and widely used in instrumentation, voice and audio applications, featuring low-frequency and high-resolution. The reason behind this is because high resolution of sigma-delta ( $\Sigma\Delta$ ) architecture is obtained through trading off speed of modern CMOS (or BiCMOS) technology for high accuracy. With the continuing scale down of CMOS technology feature size and ever increasing operation speed, as well as architectural advances,  $\Sigma\Delta$  A/D converters could work at higher frequencies up to several hundred to few Ms/s Nyquist rate. The large market need for wireless and internet applications are main and overwhelming drive for the research and development of higher speed  $\Sigma\Delta$  A/D converters. The bandwidth and resolution requirements of some sample communication applications are shown in Table I.

Application	GSM / DCS1800 / PCS1900	DECT	802.11	ADSL
Bandwidth	100 kHz	700 kHz	500 kHz	1.1 ~ 5 MHz
Dynamic Range	86 dB	72 dB	76 dB	72 ~ 84 dB
Power Cons.	Minimize			

Table I, Summary of A/D converter design requirements

	Reference	Year	Technology	Architecture	BW (Hz)	Bit #	SNR (dB)	Dyna. Range (dB)	Power Cons. (W)	Vsu p (V)
SC	Brooks97	1997	0.6 $\mu$ CMOS	$\Sigma\Delta$ pipeline	1.25 M	16	89		550 m	5
	Feldman98	1998	0.72 $\mu$ CMOS	2-2-2(3-level)	700 K	13	72	77	81 m	3.3
	Geerts99	1999	0.5 $\mu$ CMOS	2-1-1	1.1 M	15	87	92	200 m	3.3
	Morizio00	2000	0.35 $\mu$ CMOS	2(1b)-2(5b)	1.1 M	14	81		99 m	3.3
				2-2-2 (all 1b)			86		150 m	
Yin94	1994	2 $\mu$ BiCMOS	2-1-1	750 K		92	97	180 m	5	
CT	Breems99,00	1999	0.35 $\mu$ CMOS	4 <sup>th</sup> -order, CT	100 K		82		1.8 m	2.5
	Koch86	1986	3 $\mu$ CMOS	2 <sup>nd</sup> -order, CT	120 K	12	77		15 m	5
	Luh98	1998	2 $\mu$ CMOS	2 <sup>nd</sup> -order, CT	1 M			50 dB	15 m	

Table II, Comparison of high speed  $\Sigma\Delta$  modulator for communication applications

Most of the  $\Sigma\Delta$  modulators were implemented using switched-capacitor circuits. In [Yin94], Yin and Sansen proposed a three-stage fourth-order (2-1-1) topology which was implemented with BiCMOS switched-capacitor circuits. Later in [Feldman98], Feldman, Boser, and Gray designed and implemented three-stage, sixth-order (2-2-2)  $\Sigma\Delta$  modulator in 0.72  $\mu$ m CMOS technology with 1.4 Ms/s Nyquist rate and

77 dB dynamic range, dissipating 81 mW with 3.3 V supply. Recently, Geerts *et al* [Geerts99] achieved 92 dB dynamic range with 2.2 Ms/s Nyquist rate, consuming 200 mW with 3.3 V supply voltage using 2-1-1 architecture. A most recent implementation is [Morizio00], two 14-bit  $\Sigma\Delta$  modulators were implemented with 2.2 Ms/s Nyquist rate consuming 99 mW (for 2-2 fourth-order cascaded structure ) and 150 mW ( for 2-2-2 sixth-order ) respectively.

The above implementations of high speed  $\Sigma\Delta$  modulators for communication applications all used switched-capacitor technique. For continuous-time  $\Sigma\Delta$  modulators, the first attempt for ISDN application was made in 1986 by Koch [Koch86]. A second-order continuous-time  $\Sigma\Delta$  modulator was designed using 3  $\mu\text{m}$  CMOS technology, with 240 Ks/s Nyquist rate, 12 bits resolution, and 15 mW power consumption in 5V supply voltage. In [Luh98], Luh *et al* presented a second-order 50 dB dynamic range continuous-time  $\Sigma\Delta$  modulator with 2 Ms/s sample rate and 15 mW power consumption. A most recent continuous-time fourth-order  $\Sigma\Delta$  modulator was designed with 100 KHz bandwidth 82 dB SNR and only 1.8 mW power consumption at 2.5 V supply voltage. Table II summarizes the state of the art of high speed  $\Sigma\Delta$  A/D converters.

## Background of the Group

There are 5 professors, more than 20 Ph.D. students, and around 40 M.S. students at our Analog and Mixed-Signal Center. We are currently working on various analog and mixed-signal projects, such as, data converters, filters, LNAs, VCOs and so on.

## Project Description

As shown in Table I, the most stringent requirement for the A/D converter comes from ADSL, the design target for the  $\Sigma\Delta$  A/D converter, using continuous-time circuitry and high-order multi-bit architecture, is summarized in Table III, which is preliminary target for this Ph.D. research.

Technology	0.5u CMOS with linear resistor and capacitor
Architecture	Continuous time 3 <sup>th</sup> -order single loop 5 bit quantizer and DAC ( which is linearized through continuous current calibration ), input stage is active-RC integrator and others stages are gm-C or active-RC integrators
Nyquist Rate	2.2 Ms/s
Oversample Factor	16~32
SNR ( signal/noise ratio )	> 72 dB
DR ( dynamic range )	> 78 dB
Power supply	3.3 V
Power consumption	< 100 mW

Table III, Design target for the continuous-time multi-bit  $\Sigma\Delta$  modulator of this research

To achieve above design target, a preliminary  $\Sigma\Delta$  architecture is proposed, as shown in Fig. 1, which has 3 stages of integrators, various feedforward and feedback paths, a multibit quantizer and two DACs.

There are several features of innovation in this architecture,

- Multi-bit (5-bit) quantizer and DAC are chosen to achieve higher resolution and less clock jitter sensitivity
- NRZ (non-return-to-zero) and DRZ (dual-return-to-zero ) pulse shaping are used to lower clock jitter sensitivity
- A new loop filtering structure is proposed to eliminate the performance degradation due to non-zero loop delay
- Current calibration is used to linearize DAC

- Digital auto-tuning could keep RC product constant while having higher linearity

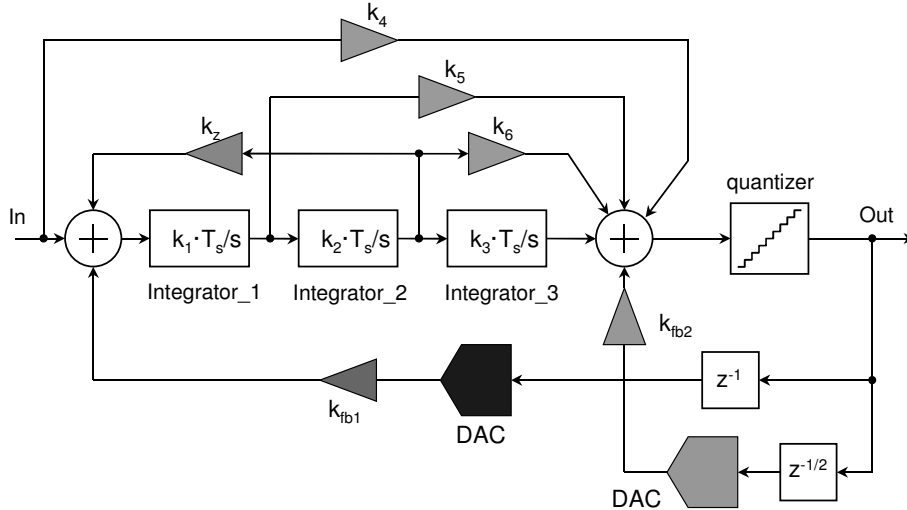


Fig. 1, Proposed continuous-time sigma-delta modulator architecture

## Simulation and layout plans

First, the system level design is carried out by using Matlab and SIMULINK. The goal is to decide the best  $\Sigma\Delta$  architecture and design parameters for the building blocks. Various non-idealities will be modeled in SIMULINK, such as, noise, nonlinearity, mismatch, and process variations. In this level, various design parameters, such as, slew rate, linearity, noise, and so on, of the building blocks will be determined.

Then, macromodel design of system is built up at Cadence and simulated. Note that, building blocks of the macromodel design have one-to-one correspondence to the final transistor level design. At the same time, transistor level design of various building blocks are carried out to satisfy the design specifications which were got from the system level design phase. And then, the transistor-level building blocks will replace the macromodel building blocks one by one. If some thing goes wrong, the design specifications will be checked and verified. At this phase, the difference between required specifications and simulated results should be justified.

Monte Carlo simulation is also required to ensure that the design is robust enough to meet the design specifications under manufacturing process variations. This will provide us with an estimated distribution of the values of the most important design specifications as a function of the statistically varying device model parameters. A buffer will be placed at the nodes we may want to test to ensure the building block is working correctly. Each block will be tested independently. The effects of bondwire, package, and parasitic capacitance caused by the interconnections will be taken into account, which is done by proper modeling.

Next, a layout of the final design will be created using Virtuoso Environment of Cadence. Proper layout techniques such as common-centriod arrangements and summy transistors should be used for better matching. The LVS ( Layout vs. Schematic ) checker tool of Cadence will be used to ensure that both the extracted layout and the schematic are matched. Postlayout simulation including all of the parasitics will be do to make sure the circuits could work properly after layout phase.

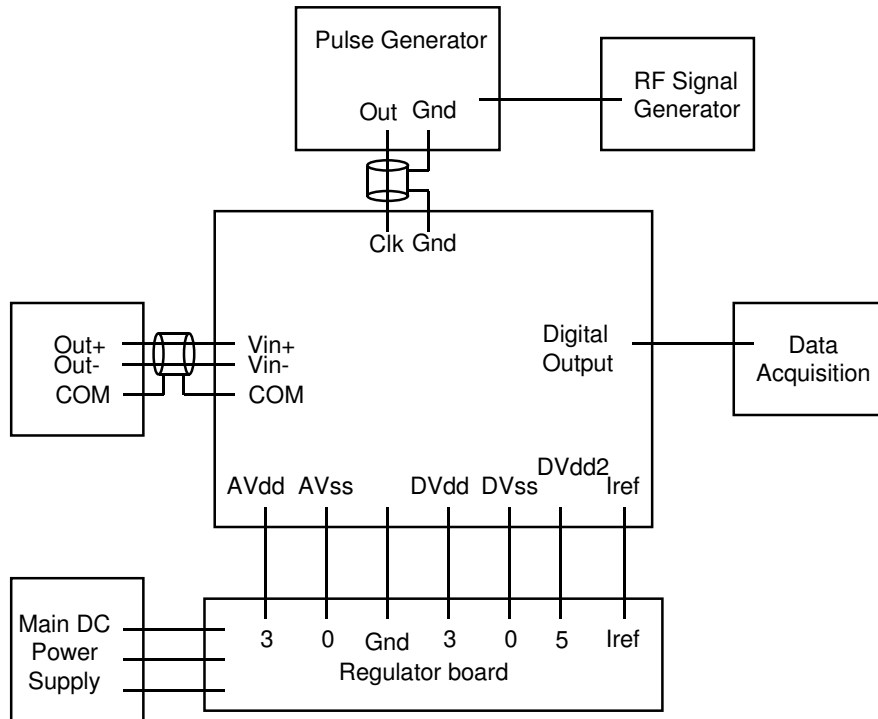
It is also important to mention that we are also intending to include in our layout, beside the main design, a bank of single transistors of different sizes. This will allow us to extract the most important model parameters ( such as the intrinsic transconductance parameters and threshold voltages ) through testing measurements and compare them with the ones provides by MOSIS.

## Test Plans

The final phase will be the characterization of the fabricated chip. A careful setup for the measurements is need.

A careful designed PCB will be used to fully characterize the fabricated chip. The preliminary test setup is shown in Fig. 2. The test board will be a two-sided, copper-clad board with separate analog and digital ground planes that are connected together at the power supplies. The supply pins will be bypassed by 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$  ceramic surface-mount chip capacitors in parallel.

The group has a probe station that will be used to test some unpackaged samples of the chip allowing us to obtain more accurate measurements of the circuit performance.



## Milestones and Deliverables

The milestones and deliverables are shown in the following table.

	05/01	06/01	07/01	08/01	09/01	10/01	11/01	12/01	01/02	02/02	03/02
Architecture design	X	X									
Building block design		X	X	X							
System integration				X	X	X	X	X			
Test procedure								X	X		
PCB for testing										X	X
Report on measurement											X
Progress report	X		X		X		X		X		X

Table IV, Milestones and deliverables

## Estimated Projects Size

Since we are planning to integrate two different architectures on the same chip, the required silicon area is large. Besides, we will fabricate some building blocks independently, which may even double the required area.

We may send several smaller chips with building blocks for fabrication, and then one or two bigger chips with the whole system. The total estimated silicon area for this project is 4mm x 4mm, which is the total area of several chips.

## Student involved

Shouli Yan  
Bo Xia

## Professors involved

Dr. Edgar Sánchez-sinencio

## References

- [Breems99] Lucien J. Breems, Eric J. van de Zwan, E. Carel Dijkmans, and Johan H. Huijsing, "A 1.8 mW CMOS sigma-delta modulator with integrated mixer for A/D conversion of IF signals," *ISSCC 1999*, pp. 52-53, 1999
- [Breems00] Lucien J. Breems, Eric J. van de Zwan, and Johan H. Huijsing, "A 1.8 mW CMOS sigma-delta modulator with integrated mixer for A/D conversion of IF signals," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 468-475, April 2000
- [Brooks97] T. L. Brooks, D. H. Robertson, D. F. Kelly, A. Del Muro, and S. W. Harston, "A cascaded sigma-delta pipeline A/D converter with 1.25 MHz signal bandwidth and 89 dB SNR," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1896-1906, Dec. 1997
- [Feldman98] A. R. Feldman, B. Boser, and P. R. Gray, "A 13-bit, 1.4-MS/s sigma-delta modulator for RF baseband channel applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 10, pp. 1462-1469, Oct. 1998
- [Geerts99] Y. Geerts, A. M. Marques, M. S. J. Steyaert, and W. Sansen, "A 3.3-V, 15-bit, delta-sigma ADC with a signal bandwidth of 1.1 MHz for ADSL applications," *IEEE J. Solid-State Circuits*, vol. 34, no. 7, pp. 927-936, July 1999
- [Koch86] R. Koch, D. Heise, F. Eckbauer, E. Engelhardt, J. A. Fisher, and F. Parzefall, "A 12-bit sigma-delta analog-to-digital converter with a 15-MHz clock rate," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 6, pp. 1003-1010, Dec. 1986
- [Luh98] L. Luh, J. Choma, Jr, J. Draper, "A 50-MHz continuous-time switched-current sigma-delta modulator," *IEEE ISCAS 1998*, vol. 1, pp. 579-582, 1998
- [Morizio00] J. C. Morizio, M. Hoke, T. Kocak, C. Geddie, C. Hughes, J. Perry, S. Madhavapeddi, M. H. Hood, G. Lynch, H. Kondoh, Kumamoto, T. Okuda, H. Noda, M. Ishiwaki, T. Miki, and M. Nakaya, "14-bit 2.2-MS/s sigma-delta ADC's," *IEEE J. Solid-State Circuits*, vol. 32, no. 7, pp. 968-976, July 1997
- [Yin94] Guangming Yin and W Sansen, "A high-frequency and high-resolution fourth-order sigma-delta A/D converter in BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 29, no. 8, pp. 857-865, Aug. 1994