Design of an Optical Intensity Comparison Pixel with Programmable Intensity Offset Levels

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1. Introduction

Optical interconnect arrays, developed with the help of wave-guides and semiconductor interconnections, form a primary aspect of any optoelectronic network. These form the basis for a wide variety of operations that could be performed on a series of optical signals, paving the way for a whole new dimension in mixed-signal computations. Conceivably, arithmetic and simple logic operations [1] (such as sorting, ranking and comparing) may be accomplished using these arrays. This project is an attempt to design and implement a smart-pixel system capable of comparing two analog signals after compensating for the interconnect losses incurred by each signal. Such a pixel has useful applications in analog ranking and sorting systems mentioned above. These systems provide for parallel comparison and ranking, unlike conventional digital sorting/ranking algorithmic implementations, which are usually more than linearly dependent on the number of inputs.

2. Project Description

The pixel has been designed to receive the two signals from two separate photoreceivers [2], which detect the corresponding optical signals and convert to them to an equivalent electrical one for subsequent processing by the pixel, and then compare the two signals after accounting for the intensity loss due to attenuation at each tapping the signal has traversed. For this purpose, the pixel has to generate an offset signal dependent on the positional coordinates of the pixel in the array as well as the attenuation occurring at each interconnect. The flexibility of the pixel has been enhanced by incorporating the ability to vary the offset signal by programming it for different values of the attenuation coefficient. The coordinates of the pixel in the array (in the form of two 4-bit binary numbers) are stored in two registers, while a voltage corresponding to the attenuation factor at each interconnect) is fed into the pixel as an analog dc level (100% attenuation corresponding to the maximum voltage swing of the chip). The pixel is capable of generating an offset voltage based on these data, which is then multiplied to the respective signal before comparison.

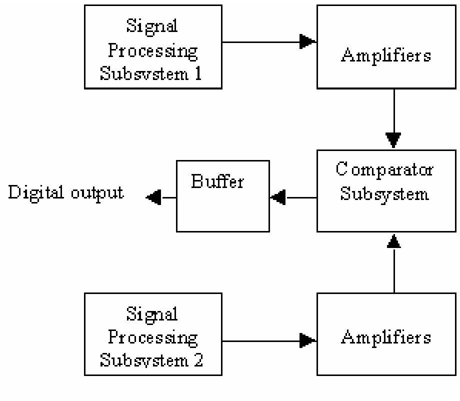

Fig 1a: Block diagram of the entire system

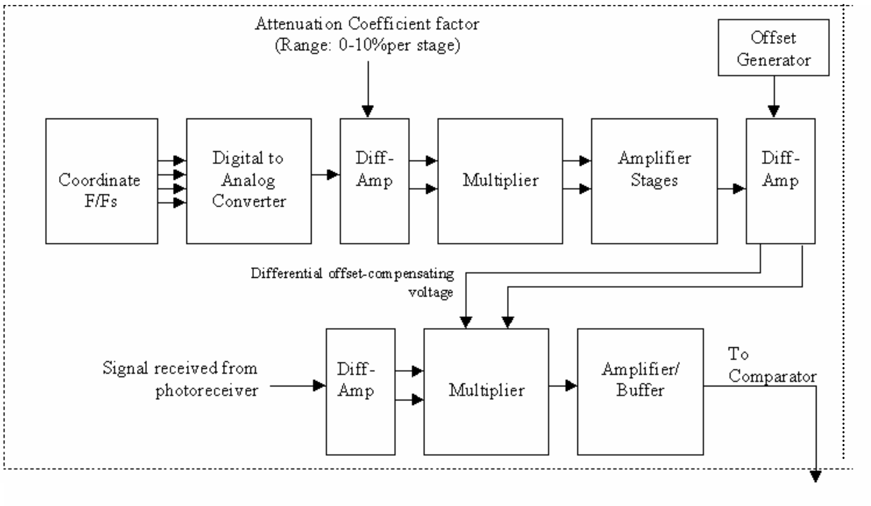

Fig 1b: Detailed view of a single Signal Processing Subsystem

The block diagram of the entire pixel is shown in Figs.1a and 1b. It consists essentially of two broad subsystems:

1. Two separate signal-processing subsystems, which receives each optical signal, converts it into an electrical analog, and adds the correct offset to it in order to compensate for the interconnect losses.
2. The comparator subsystem, which compares the two compensated analog signals, and produces a digital voltage based on the result of the comparison. In other words, it determines whether one signal is greater than the other.

The signal-processing subsystem involves the reception of the signal, and its subsequent processing to compensate for the interconnect losses in the grid array. The offset voltages are calculated separately by converting the digital coordinates into their analog equivalents and then combining them with the attenuation coefficient value, which is taken as a fractional input to the total voltage range of the chip (5V). Since analog computations involving variable exponents are difficult and inaccurate to implement in CMOS technology, a linear approximation method has been adopted for the calculation of the offset voltage. In this method, the exponential variation of the offset with the value of the positional coordinate has been approximated as a linear variation, with the assumption that the attenuation at each stage is only a very small factor of the total intensity of the signal. This reduces circuit complexity enormously, while playing an important part in accentuating the resolution of the system (by introducing linearity in operation). For large values of the attenuation coefficient, where the linear approximation fails, the inherent non-linearity of the circuit at the digital-to-analog converter and the following amplifier stages have been taken advantage of, in order to introduce a slightly quadratic trend in the output signal instead of a perfectly linear one. This has resulted in a more accurate determination of the offset voltage generated, and matches closely to the expected values, as demonstrated in the simulation results discussed in the following section.

A pair of analog multiplier assemblies then multiplies the offset voltage so generated with their respective received signals. The signal so generated is proportional to the actual signal intensity before it entered the wave-guide array. These signals are then amplified and compared at the comparator subsystem. The result of the comparison process is a digital signal, which is subsequently passed through several stages of buffers to adjust voltage swing and timing synchronizations for input into following digital circuits.

The present work finds use not only in the mentioned application, but also in all mixed-signal systems where signal attenuation plays an important role in system performance. Its simplicity and compact implementation allows it to be easily incorporated into any system as a stand-alone module, and is also compatible with digital systems since the circuit has been designed to operate with a 0-5V power supply, just like normal digital systems. The current capacity of the pixel has been so adjusted that it can be used as a direct input to a digital system.

3. Simulation Plans

The entire pixel has been designed and simulated with T-Spice, a circuit simulation tool by Tanner Tools. The simulation results reveal that the offset voltage has a dc characteristic that is highly linear with deviation from expected values less than 3% over most of the range of the coordinate value and attenuation coefficient (except for very low values).

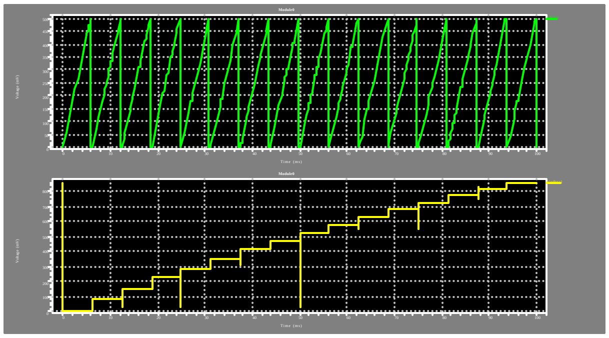

Fig. 2a: Simulation inputs for the analysis of the error voltage. For each value of the coordinates (output of the D/A converter is shown in the lower plot), the attenuation factor voltage (top) is swept through its entire range.

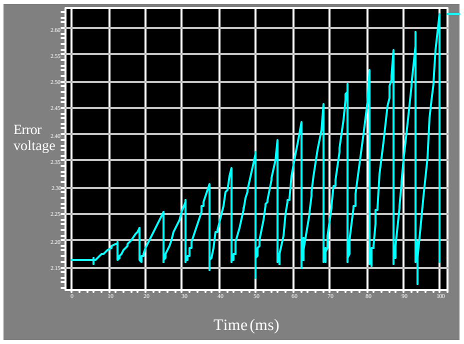

Fig. *2b: Simulation results for the error-compensating signal.*

Fig. 2b shows the generation of the linearly varying error signal for all possible values of the coordinates. For simulation purposes, the attenuation factor input voltage is swept from 0 to 10% for each value of the coordinate (Fig. 2a). This error voltage, when multiplied with the attenuated signal, gives results which have deviations of less than 5% from the expected values for large attenuation factors because of the linear approximation. Even then, the result of the comparison process does not reflect this error.

For a comparator resolution of 0.4mV(achieved during simulation), the worst-case analysis reveals that the linear approximation and its modifications provide a valid output for the attenuation at each tapping less than or equal to 10% of the total intensity. Monte-Carlo results have revealed that technology-dependent MOSFET parameter changes (the more prominent ones being the body-effect parameter, GAMMA, and the narrow channel effect on the threshold voltage, THETA) would result in deviations of about 3-7% of the total output range. This value, although substantial as compared to the resolution of the comparator, tracks each other for both signals, resulting in the compensation of the error at the comparator stage. The average power consumption of the circuit is about 2.1mW, with a peak power of 3.4mW.

4. Project Size

The entire pixel has an area of 291,033.6μm^2 (528μm * 551.2μm). However, for the prevention of excessive and asymmetrical loading at the output of the different stages of the circuit connected to the test pins, more than one circuit have to be placed in the chip. Also, the added test structures like amplifier stages and current mirrors would require an entire chip size of 2.2mm * 2.2mm. The chip has been designed to be fabricated in the AMI-ABN 1.5μm process.

5. Test and Characterization Plans

The testing strategy is to load just a single stage at a time by connecting it to the output pins, so as to prevent the intermediate stages to be loaded too much to cause substantial deviations or time delays at its output. Also, the same inputs would be supplied to the different circuits, so that all the intermediate stages for a given set of inputs may be determined and tested simultaneously. All control signals would be swept through its entire range of allowed values, determined by simulation results, and the corresponding output pattern would be compared to simulation results. This would result in exhaustive testing of all possible results. Testing of intermediate stages would be done for both processing subsystems simultaneously to prevent asymmetrical loading of the two stages, which could result in erroneous comparison. Also, independent amplifiers and current mirrors are to be incorporated into the chip, and tested separately from the actual pixel, to determine the difference in performance when placed in the circuit, and the effect of loading effects. Finally current measurements would be performed on each pixel for power estimation.

6. Milestones

Commitment	Date of Completion
Pixel Layout and Simulation	11/01/2001
Chip layout and debug	02/01/2002
Submission to MOSIS	02/05/2002
Receive chip from MOSIS (tentative)	04/05/2002
Testing	05/01/2002
Results/ Feedback to MOSIS	06/01/2002
Report	07/01/2002

7. References

1. Allen, P.E., Holdberg, D. R., *CMOS Analog Circuit Design.* New York, NY, Holt, Rinehart and Winston, Inc., 1987, pp. 95-98, 273-299, 327-356, 591-607, 521-548.
2. J. Tang, S. Konanki, B. Seshadri, B. K. Lee, R. C. J. Chi, A. J. Steckl, and F. R. Beyette, Jr., "*CMOS photodetectors/receivers for smart-pixel based photonic systems*," in Proceedings of SPIE, vol. 4109, pp. 75-82, SPIE Conference on Critical Technologies for Future Computing Systems, San Diego CA, July - August, 2000.