

Low-Voltage and Low-Power Analog Front End in a Deep-Submicron Digital Process

Keith Kraver and Prof. Richard B. Brown

Key to the success of portable electronic devices and other related consumer products is the reduction of manufacturing cost, size, weight, and power consumption (for extended battery life). The levels of integration afforded by current and future silicon processes promotes a system-on-a-chip (SOC) design style, which has the potential to improve all four constraints. Accordingly, the Semiconductor Industry Association (SIA) predicts that SOC design, with differing design styles including analog, mixed-signal (analog and digital), RF, and microelectromechanical systems (MEMS) will be one of the five difficult challenges to be addressed before 2005. Due to oxide reliability constraints, the SIA also predicts that supply voltage will drop to 900mV by 2009. In addition, batteries limit the miniaturization of and are a substantial determinant of the cost and weight of the total system. A significant savings in cost, size, and weight is realized when portable devices can function with only a single cell down to the end-of-life voltage, around 900mV for typical battery technologies.

SOC integration requires that analog and digital circuits are designed in the same process and share a common substrate. Processing advancements enabling smaller features improve the performance (notably speed and power dissipation) of digital circuits. Analog circuits, however, tend to experience a degradation in performance due to specific processing characteristics and the reduction of the supply voltage. In this project we are exploring low-voltage and low-power analog and mixed-signal circuit design in deep-submicron digital processes through the design of analog front ends (AFE) for single-chip instrumentation systems. The first design (3V, 0.35 μ m CMOS) integrates a temperature sensor, several sensor interfaces, amplifiers, and data conversion with a custom microcontroller. This design, referred to as the MS-8, was fabricated through National Semiconductor and was an award winner in the 2000 DAC design contest. The current AFE (900mV, 0.18 μ m CMOS) to be submitted to MOSIS for the TSMC 0.18 μ m fabrication run consists of input voltage buffers, a programmable gain amplifier, and a second-order sigma-delta ADC.