MOSIS Education Program RESEARCH Account Proposal

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Project Title: The Analysis and Modeling of Dual-Gate MOSFETs

Requested Fabrication Technology: TSMC 0.25 μm

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1 Project Description

The dual-gate MOSFET (DGFET) devices have an extensive use in MOS integrated circuits because of their functional properties such as modulation of the channel current, charge transfer through the channel for RAM applications or mixing and multiplication capabilities. One can make use of these devices for a range of applications where electronic gain control, low feedback parameters, low noise, cross modulation or reduction of short channel effects is a requirement [1], [2]. These devices can also be used in applications demanding compact, device-scale multiplicative properties, like in the case of neural networks and similar parallel processing systems.

Athough these devices have found themselves a variety of application fields, there is still a need for an analytical model which will define the DGFET behavior explicitly. Such a model requires a more careful and detailed analysis than it does for the modeling of the single gate MOSFET, because of the device structure and the interactions between the controlling gates.

The aim of the project is to derive an explicit analytical model, to be generalized for dual and multi-gate MOSFET structures, with well-defined parameters required for the circuit simulations. Such an analytical model will allow the simulation and the small signal characterization of these devices in the circuit simulators at the design stage. The model can also be used to derive the small-signal behavior of these devices in an analytical fashion. Therefore the related parameters, and the nonlinear modulation effects of the device can be expressed in well-defined forms. The results of this model should be compared with the physical device behavior. For this purpose a test chip with DGFET structures of different geometry and size is proposed.

The adjacent gates of a DGFET device should be very close to each other for proper device operation. This is necessary for a strong interaction of the electrical field of the gates, hence for the proper device operation. This requirement can only be achieved by making adjacent poly-gates as close as the technology admits. Therefore the test chip is proposed to be fabricated with the TSMC 0.25 micron deep-submicron process. Several sample DGFET devices will be put in the layout for changing gap lengths, and for different gate lengths and widths. The characteristics of these devices will be measured in order to form a basis for the theoretical results.

2 Estimated Project Size

The estimated chip size is that of Tanner Hi-ESD minimum pad frame, for TSMC 0.25 μm technology (1.5 mm x 1.5 mm or 12500x12500 λ^2, λ=0.12 μm).

3 Simulation, Test, and Characterization Plans

The numeric simulation of the devices is carried out by using the PISCES device simulator program, considering the two-dimensional field effects of the gates along each other for DC operation. The test and characterization will cover the measurement of DC characteristics for the sample devices, for different bias conditions and for different geometries. The biasing parameters are namely the gate1, gate2 and drain voltages. From the measurement data, the I-V characteristics of all the devices will be carried out. Then these data will be compared with the estimations of the theoretical results. An agreement in the measurements and theory will lead us to define a general analytical model to be used in the simulations. Such an improvement will ease the design stage considerably, which is very important, especially for a large-scale application including DGFETs. It is also possible that new capabilities of this device can be obtained from the theory and the measured data, and the application area for DGFET device can further be extended.

References

[1] Barsan R.M., "Analysis and Modeling of Dual-gate MOSFETs", *IEEE Transactions on Electron Devices,* Vol. ED-28, No. 5, pp. 523-534, May 1981.

[2] Barsan R.M., "Subthreshold Current of Dual-Gate MOSFETs", *IEEE Transactions on Electron Devices,* Vol. ED-29, No. 10, pp. 1516-1521, October 1982.