DESIGN FOR MOSIS EDUCATIONAL RESEARCH PROGRAM

IMPROVEMENT OF CMOS MAGNETIC FIELD STRUCTURES AND FRONT-END CIRCUITS

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Abstract

The CMOS magnetic field structures and front end circuit design was implemented on CMOS AMI C5F process. The submitted design contains Hall structures, interface and bias polarization circuits. The whole project is enclosed in 1.69 mm x 1.69 mm area with 24 pads. The aim of the project is centered on the evaluation of the sensor sensitivity in order to obtain the viability of the design for biological applications. Special care must be had the noise and the temperature variations. The following sections describe each part of project.

Project Description

Hall structures

The magnetic field structures based on Hall effect is regarded on the interaction between moving electric carriers (inside of the flat conductive strip and from control terminals) and an external magnetic field (vector B is perpendicularly to the structure) [1]. The strip has a length and width, L and W respectively. The Hall structure is enclosed in a four-terminal rectangle (two bias or control terminals and two sensing contacts). The strip has the two sensing contacts, S₁ and S₂ at its left and right sides of structure (orthogonally to control terminals). The magnetic field is detected by the potential difference between S₁ and S₂ contacts (voltage known as Hall voltage). The control current (or control voltage) is applied between bias control terminals. The control current is preferred because the temperature variations diminished.

The Hall voltage is proportional to the perpendicular magnetic induction, the bias current supplied and the geometric correction factor. This factor approaches to the unity for the limit of the infinitely long Hall strip [3]. A large variety of analytical works for rectangular, circular, octagonal are available. A summary of these calculates the factor close to the unity for long rectangular plate with ratios of $L < W$ and $L/W > 1.5$. The analytical simulations give the geometric correction factor behavior related to long and width dimensions as is shown in Figure 1.

![Figure 1](image)

In order to evaluate the geometric correction factor (shape effects) a different ratios of $L/W$ and $S/W$ was incorporated. A several combinations of these ratios will be designed. The methodology for the comparison will be as is showed in Table I. The structures have been calculated with different length-width-ratio: 5 and 10 times, and 6 and 12 times smaller; also, the calculations have been done for contact-width-ratios of 16, 24, 32 and 40 times smaller. The main combinations are showed in Table 1.
### Table 1. Ratio combinations of length-to-width ratio and contact-width-ratio.

<table>
<thead>
<tr>
<th>width-to-length ratio</th>
<th>contact ratio</th>
</tr>
</thead>
<tbody>
<tr>
<td>L/W_b &lt; L/W_c</td>
<td>S/W_b = S/W_c</td>
</tr>
<tr>
<td>L/W_a = L/W_b</td>
<td>S/W_a &gt; S/W_b</td>
</tr>
<tr>
<td>L/W_b &lt; L/W_d</td>
<td>S/W_b &lt; S/W_d</td>
</tr>
</tbody>
</table>

Additional typical structures were designed in order to estimate the dependence on magnetic force straight lines. The sensor is designed using the n-well layer (and poly layer to compare the performance) using minimum values design rules for the width and spacing. The microstructure layouts are shown in Figure 2.

![N-well structures for different dimensions.](image)

The contacts S have 3.6µm (a, b) and 4.5µm (b, d) contact dimensions. Analytical simulations were carried out in order to estimate the dependence of the behaviour on magnetic field B_z, control current I_{bias} and Hall voltage V_{Hall}. The data extracted from these simulations (see Figure 3) give us the bias control for the current source.

![Plot of behaviour for Hall voltage V_{Hall} on control current I_{bias} and on magnetic field.](image)

Figure 3. Plot of behaviour for Hall voltage V_{Hall} on control current I_{bias} and on magnetic field. The sweep range performed has been between 10µ to 100µ A and 0.1µT to 10 µT respectively.
The behaviour shows than for several milivolts on Hall voltage, a high control current is needed. In our case, the bias circuit has designed for handling a current of 100µA.

**Current source and amplifier designed**

The control current has been designed through current source circuit. The implementation of cascode current source increases the stability over a large output voltage range and the output impedance. The circuit is accomplished by putting three current sources in cascade to each other.

The cascode current source uses 6 N-channel MOSFET transistors. The set current is given by: \( I_{REF} = k_n \left( \frac{1}{2} V_{DD} - V_{TH} \right)^2 \), the \( I_{out} \) is equal to \( I_{REF} \) for output voltages exceeding \( V_{GS1} + V_{GS2} + V_{GS3} \). The minimum voltage output is \( 3V_{SAT} + V_{TH} \) above the rail \( V_{SS} \). This circuit has higher output impedance than the sample current mirror, but lower output swing due the extra device. The spice simulation of the current source, designed for \( I_{out} = 100\mu A \) (with \( V_{DD} \) and \( V_{SS} \) ± 2.5 V, \( V_{GS} - V_{TH} = 0.56 \) V overdrive voltage, \( V_{TH} = 0.69 \) V and \( W/L = 30 \)) has been done to describe their electrical behavior such as, static transfer characteristic. The simulation results shown the good current source behavior over a wide output voltage swing.

The signals from Hall structures have been directed outwards of chip, by the opamp. This front-end circuit consists of 10 voltage gain stage. The first stage is a differential amplifier (M1/M2, with bias current source thought M5 to M6). The second stage involves transistor M7 to M10. Transistor M11 is a final buffer (source follower) to provide reasonable output drive capability. To improve the stability of circuits, a frequency compensation block has been tied between the gate of M8 and the sources M9 and M10. Figure 4 the opamp layout.

![Figure 4. Op Amp Layout.](image)

The main result of simulation exhibits an open-loop gain of 63dB. The absolute maximum ratings are: supply voltage of 2.5 and operating temperature range between -25 to 80°C; instated the electrical characteristics are: input bias current of 60µm, common mode rejection ratio of 88dB, bandwidth of 8.1 MHz, phase margin, 46°, slew rate \( \approx 15 \) V/µs and output swing of 1.6Vp-p. The transistor aspect ratios used are listed in Table 2.

<table>
<thead>
<tr>
<th>( W/L )</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>M7</th>
<th>M8</th>
<th>M9</th>
<th>M10</th>
<th>M11</th>
<th>M12</th>
</tr>
</thead>
<tbody>
<tr>
<td>( W/L )</td>
<td>7.2/1.2</td>
<td>7.2/1.2</td>
<td>16.8/1.2</td>
<td>16.8/1.2</td>
<td>4.8/1.2</td>
<td>4.8/1.2</td>
<td>4.8/1.2</td>
<td>33.6/1.2</td>
<td>24/1.2</td>
<td>72/1.2</td>
<td>360/1.2</td>
<td>1197/1.2</td>
</tr>
</tbody>
</table>
The whole circuit is enclosed on 179µm X 94µm of die (capacitor and resistor included), instead the area of the current source is 42µm X 28µm.

Fabrication Specifications

All circuits and structures were designed using AMI 0.5µm C5F process design kit and CADENCE IC package [2]. A frame-package of 24 pins pad was considered. The measures of CMOS circuits would take place, after the microsystem has been packaged.

Test and characterization procedure

1. The current source will be measured by using CIDS laboratory equipment: Keithley model 2400 and 2440 which have voltage range of +- uV to 20V, with 10pA and 42V with 100pA resolution respectively.

2. The Hall structures and circuits will be measured using a domestic Gaussimeter.

References

