Design for MOSIS Educational Program (Research)

Transmission-Line-Based, Shared-Media On-Chip Interconnects for Multi-Core Processors

Prepared by: Professor Hui Wu, Jianyun Hu, Berkehan Ciftcioglu, Jie Xu, Shang Wang

Institution: Department of Electrical and Computer Engineering, University of Rochester

Date of Submission: April 11, 2011
Project description

With the number of cores increases, the interconnection between the cores in a multi-core processor becomes increasingly critical to its performance and energy efficiency. Packet-switched interconnect, which has been proposed to replace conventional buses, offers many advantages such as bandwidth scalability and modularity. However, it requires routers that consist of complex circuits, occupy significant chip area and consume significant power [1]. In addition, repeated packet relaying adds latency to communication, which may degrades the performance significantly [2]. In this project, we propose to explore an alternative solution for on-chip interconnect in future multi-core processors, namely, *transmission-line based shared-media interconnects* [3], which potentially can provide both large bandwidth (in tens of Tbps) and extremely low latency.

A transmission line allows speed-of-light signal propagation, which translates into extremely low latency [4], and large bandwidth, potentially providing sufficient throughput such that packet switching can be avoided [3]. We propose to use transmission lines as a shared communication medium, which is similar to a bus in terms of networking but significantly different in terms of circuit implementation, signaling, and performance. As shown in Fig. 1, the global interconnect based on this technology connects all cores in a processor, and is entirely made of a multi-drop transmission line system. Each core has multiple transceivers transmitting and receiving multi-bit data through the shared transmission lines. It is worth noting that the shared medium approach enables both point-to-point communications and broadcasting. Because of the simple bus topology, packet switching is avoided, leading to good energy efficiency and low latency. The throughput comparable to a packet-switching network can be achieved by operating the interconnect at higher data rate and by utilizing the low-latency interconnect more efficiently on the architectural level [3]. In Fig.1, for example, 16 transmission
lines are used in the global interconnect. Each transmission line operates at a data rate of 62.5 Gbps, and the whole interconnect system can achieve a total throughput of 1 Tbps. The high data rate can be achieved by using a fast communication clock frequency (40 GHz) and an M-ary coding (M=4), thanks to the good signal integrity of transmission lines. The transmission lines can achieve a low latency of 6 ps/mm, which leads to a maximum latency of less than 600 ps for communication between the communication nodes at two ends of the transmission lines (Node A and B in Fig. 1) in a 2.3-cm by 2.3-cm chip. That translates into 3 computing cycles for a 5-GHz processor, half of the time in a packet-switching mesh network.

To demonstrate this new interconnect, we propose to design and fabricate a test chip through MOSIS Education Program (Research) using IBM 130 nm SiGe BiCMOS (8HP). The high-performance transistors and metals in this process would be sufficient for the high-performance transmission lines and high-speed transceiver circuits, without committing to a cutting-edge CMOS technology. The test chip will mainly consist of a prototype processor with four nodes connected by a transmission-line based global interconnect. As shown in Fig. 1, each core has multi-bit high-speed transceivers, which includes multiple sets of transmitter and receiver. Implemented with high-speed circuit techniques, each transceiver delivers multi-bit data over shared transmission lines.

What differentiate this interconnect from conventional buses is the design of the transmission line system. Properly designed on-chip transmission lines allow low-loss, low-latency propagation of signals, exhibit small dispersion (i.e., large bandwidth), and generate less crosstalk. Note that this is different from transmission line design in microwave circuits due to the large number of transmission lines running in parallel within limited chip area. In other words, bandwidth density is the key performance target, and crosstalk likely poses the greatest design challenge. Based on our prior research on wideband on-chip transmission lines [5], we will investigate several new transmission line structures for interconnect applications, such as multilayer coplanar waveguides and strips, and optimize the design through both electromagnetic (EM) simulations and system analysis to satisfy all the requirements.

Equally important is the design of the high-speed transmitter and receiver electronics. As shown in Fig. 2,
the transmitter consists of a serializer (SER) to convert the low-speed parallel data into high-speed serial data, and a wideband driver to drive the transmission line. The receiver includes a wideband amplifier to amplify the received data, a latch sampler to sample the data and generate the large-swing output, and a deserializer (DES) to convert the received high-speed serial data into low-speed parallel data. We will take advantage of our prior research in ultra-wideband impulse radio circuits in the transceiver design [6]. A high-frequency ILO-based clock multiplier with phase tuning capability [7] to generate the required high-frequency communication clock and the optimum phase for the latched sampler. A dedicated clock distribution transmission line provides the reference clock to all the transceivers [8].

In addition, several stand-alone test circuits will be included in the test chip, such as the ILO-based clock multiplier, the transmitter driver, the receiver amplifier, and the latched sampler.

Reference:
Fabrication process:
IBM 130 nm SiGe BiCMOS (8HP).

Packaging requirements:
No. We will wire-bond the chip to a custom substrate for testing purpose.

Estimated project size (length and width):
Length: 4mm; Width: 4mm

Simulation plans:
The simulation will be performed in several domains using several industrial standard EDA tools. The transmission line will be simulated and optimized in a full-wave planar electromagnetic simulator, Sonnet. We will try to achieve lower attenuation, larger bandwidth, less crosstalk transmission lines with smaller area. The transmitter and receiver will be simulated in Advanced Design System (ADS) and Cadence Spectre in both time-domain and frequency-domain. Each individual building block will be simulated first. The design goals are high speed, low noise and low power consumption. The ILO will be optimized for better jitter performance, larger locking range and phase tuning range. Then the whole on-chip interconnect system will be simulated in ADS and Spectre. After a single transmission-line design is done, the case with multiple transmission-lines will be simulated, focusing on the crosstalk performance.

Test and characterization plans:
The prototype will be characterized in both time and frequency domain. Before the whole system characterization, each building block will be characterized first using the stand-alone test circuits. The transceiver circuits’ gain, bandwidth and noise figure will be measured, and the transmission line’s loss, dispersion, and impedance will be characterized. We will also characterize the working range, locking range, phase noise and phase tuning capability of the ILO-based clock multiplier.

For the whole system characterization, the reference clock will be provided by a signal generator to the prototype and fed to all the nodes through the transmission-line-based clock distribution network. An on-chip high-speed pseudorandom binary sequence (PRBS) generator in the transmitter will generate the data pattern for the test purpose, the output of the latched sampler in the receiver will be observed through the oscilloscope. Initially, only one data link will be activated. We will measure the highest achievable data rate, power consumption, eye diagram, latency, and bit error rate for each time. Then all data links will be used to transmit data, and we will characterize the crosstalk performance of the system.