Design for MOSIS Educational Program (Research)

This project will be composed of two parts, which will share the available area

Project Title:

Part A

“Electrical Characterization of Standard and Non-Standard Layouts for MOSFET, Focusing on the Planar Power MOSFETs and the Operational Transconductance Amplifiers (OTA)”

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Re-fabrication Request.

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**Project description**

**Part A**

“Electrical Characterization of Standard and Non-Standard Layouts for MOSFET, Focusing on the Planar Power MOSFETs and the Operational Transconductance Amplifiers (OTA)”

(Prof. Salvador Pinillos Gimenez, PhD)

Recent studies demonstrate that the planar and three-dimensional (3D) MOSFETs performances improve significantly by using of the drain-channel-source regions interfaces engineering approach, in which is based simply by changing of the gate layout [1-7] from rectangular to others gate geometrics shapes. This simple approach do not causes any extra burden to the current integrated circuits (ICs) CMOS manufacture process [1-7] and also can further help to extend the lifetime of the current planar CMOS manufacture process. There are several examples of MOSFETs that use this approach, as for example the CIRCULAR GATE MOSFET (CGM) [1], the OVERLAPPING-CIRCULAR GATE MOSFET (O-CGM) [2], the WAVE MOSFET (WM) [3-4], the DIAMOND MOSFET (DM) [5], the OCTO MOSFET [6] and the FISH MOSFET (FM) [7].

The CGM can operate in two different operation modes: internal and external drain bias configurations. When the CGM operates as internal drain bias configuration, this device is able to improve the drain current ($I_{DS}$), transconductance ($g_m$) and on-state drain to source series resistance ($R_{DS,ON}$) than those observed when it is biased in the external drain bias configuration and therefore it is an alternative device to be used mainly as switch and buffer in ICs digital applications and also as input stages of operational transconductance amplifiers (OTAs) in analog ICs applications [1]. Figure 1 shows two circular gate nMOSFETs layouts, where the internal contact can operate either as a drain (Figure 1.a) or as a source (Figure 1.b).

Figure 1: Example of the circular gate nMOSFET layouts, where the internal contact can be operate either as a drain (1.a) or as a source (1.b).

The O-CGM was specially designed in order to improve the integration factor $[(W/L)/A$, where $W$ and $L$ are respectively the channel width and length and $A$ is the MOSFET silicon area] of the planar power MOSFETs (higher W/L), as indicated in the Figure 2 [2].
Figure 2: Example of an Overlapping-circular gate MOSFET layout, where \(a_{\text{msk}}\) and \(b_{\text{msk}}\) are respectively the internal and external radius of the gate region and \(\alpha\) is the contact angle between two or more O-CGMs.

The Wave SOI MOSFET was specially designed to transform a CGM in a symmetric device regarding the source and drain regions. It presents the same aspect ratio \((W/L)\) than the one found in the CGM and presents a higher integration factor \([(W/L)/A, \text{where } A \text{ is the transistor silicon area}]\), as indicated in Figure 3 [3-4].

Figure 3: Example of a Wave SOI MOSFET layout.

The Diamond layout style (Figure 4) was specially designed to present a hexagonal geometric shape of the gate in order to use the corner effect in the longitudinal direction of the channel region. This effect is defined as a Longitudinal Corner Effect (LCE) and it is capable to increase the longitudinal resultant electric field along of the channel \((\vec{E}_l)\), given by \(\vec{E}_l = \vec{E}_{1/l} + \vec{E}_{2/l}\), and consequently improve the mobile carriers average velocity along of the channel \((\vec{u}_l)\) and therefore it is able to improve \(I_{DS}, g_m, g_m/I_{DS}, R_{DS, ON}\) [5].

Figure 4: Example of an Diamond SOI nMOSFET (DSM) layout style.

In Figure 4, \(t_{\text{ox}}, t_{\text{SI}}, t_{\text{BOX}}\) are respectively the gate oxide, silicon film and buried oxide thickness and \(b\) and \(B\) are the smaller and higher dimensions of the gate length of the DSM.

OCTO SOI MOSFETs (Figure 5) is an evolution of the Diamond SOI structure and it presents an octagonal gate geometry in order to enhance the breakdown voltage \((BV_{DS})\) and Electrostatic Discharge Effect robustness [6].

Figure 5: Example of an OCTO SOI MOSFET (DSM) layout style.
The longitudinal resultant electric field along of the channel \( \vec{E}_L \), given by \( \vec{E}_1 \vec{E}_2 + \vec{E}_3 \), and consequently further improve the mobile carriers average velocity along of the channel \( \vec{E}_L \) and therefore it is able to further improve \( I_{DS} \), \( g_m \), \( g_m/I_{DS} \), \( R_{DS,ON} \) as compared to the Diamond layout MOSFET (DSM) [6].

Finally, FISH SOI MOSFET (FSM) is also an evolution of the DSM and it is specially designed to digital integrated circuits applications. It presents a gate geometric shape like a “smaller than” mathematic symbol (<) and can be manufactured with the minimum dimension \( L_{min} \) allowed by the CMOS process, as illustrated in Figure 6. It preserves the LCE along of its channel length, in which it is presented in the DSM, and consequently, the FISH layout style, for the first time, can reduce the die area of the digital integrated circuits [7].

In Figure 6, \( \vec{E}_L \) is the resultant longitudinal electric field along of the channel \( = \vec{E}_1 + \vec{E}_2 \), where \( \vec{E}_1 \) and \( \vec{E}_2 \) are respectively the longitudinal electric field components, respectively.

So, the objective of this MOSIS project is to study how these different layouts styles can benefits the planar power MOSFETs (several planar MOSFETs associated in parallel to produce high aspect ratio) [2] in terms of die area reduction, drive current in the triode and saturation regions, transconductance, Early Voltage \( V_{EA} \), \( BV_{DS} \) and \( R_{DS,ON} \), as compared to the standard layout structure, considering the same aspect ratio and bias conditions.

Different MOSFET layouts (standard and non-standard) will be using to implement different OTA layouts in order to quantify the waste die area and the electrical performance of these analog build block.

**Acknowledge**
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**Fabrication process:**

- Technology Code: 8HP SiGe BiCMOS Process;
- Date: March 31 2014;
- Estimated project size (length and width): 4000 μm x 4000 μm;
- Packaging requirements: we do not need to pack the chips;
- Quantity Unpackaged: 40;
- Simulation plans: the SPICE simulations are performed when we have the design kit of theses devices and circuits;
- Test and characterization plans: in the moment we receive the chips, we will start to perform the electrical characterizations of the devices and circuits.

**References**