July 12, 2001

The MOSIS Service  
USC Information Sciences Institute  
4676 Admiralty Way, 7th floor  
Marina del Rey CA 90292-6695

Subject: Proposal for fabrication of leakage controlled 0.25u SRAM

This proposal requests funding for the fabrication of a leakage-controlled 0.25u SRAM design which was designed by students Hai Li and Amit Agrawal to satisfy requirements for a semester project in EE695K Advanced CMOS VLSI Design. The purpose of this particular project is to evaluate the performance, dynamic power, standby power, and area overhead trade-offs associated with the application of gated-ground leakage control. Fabrication of this design in a deep sub-micron process such as 0.25u will not only serve to validate this leakage control technique – it will also test the accuracy of the available simulation models, technology files, extraction tools, and simulators as we compare results for leakage, performance, and dynamic power consumption.

Proposed Design

The chip to be fabricated includes two 4K SRAM caches. One is a conventional SRAM. The other employs a gated-ground technique, which can greatly reduce leakage in the cache's unused sections. This novel SRAM design is compatible with current SRAM design. The primary change is the addition of gated-ground transistors at the edge of the layout. The gated-ground transistors are controlled directly by the row decoder.

Our aim is to get the best trade-off between energy and performance in our gated-ground SRAM design. In order to maintain high performance, we will choose the size and threshold voltage of gated-ground transistors carefully. In the design, we isolate the gating transistors using a deep-nwell, so that the substrate bias can be controlled independently. In addition, the gating transistors will be partitioned into groups operated by separate control signals to allow us to evaluate performance and leakage control for a range of effective leakage control transistor widths.

The total area of the chip will be approximately 6 mm² with an aspect ratio on the order of 2 to 1.

Simulation and Verification Plan

Except for I/O and power bonding pads, the chip is entirely a full custom design for which schematics and cell layouts were prepared using Cadence Virtuoso. I/O and power bonding pads were taken from the LEDA Systems 0.25u library. A Dracula LVS was performed to verify consistency between the schematics and layout. Functionality of the schematic and layout was verified by simulation in HSPICE. Benchmark performance, power dissipation, and leakage control were evaluated in HSPICE using the layout netlist. Dracula DRC checks, including antenna rules, were run on the final layout and violations were corrected.

Before evaluating power dissipation in HSPICE, architecture level simulations were performed in order to determine memory activity and predict energy savings. SimpleScalar-3.0 was used to
simulate L1 and L2 data and instruction cache in the context of an out-of-order microprocessor for getting the cache utilization. Predicted energy savings were calculated using results from the SPEC95 benchmarks. Our results show that we save around 40% to 45% energy in iL1, 40% to 70% in dL1, and even more in L2 cache.

Test Plan

Testing of the SRAMs will include functional verification, performance testing, and static power measurements. Equipment available for this testing includes:

1. A Tektronix TLA 720 Benchtop Mainframe with 136 bit wide logic analysis and 128 bit wide pattern generation. The unit supports 268MHz pattern generation and 200MHz state acquisition (400MHz data rate) if only half the channels are used.
2. A Tektronix DG2040 two channel 1.1GBs data generator for use in ultra high-speed testing.
3. An Agilent 86100A digital oscilloscope with 20GHz sample rate input modules, for use on ultra high-speed tests.
4. A Keithley 6430 Sub-Femtoamp SourceMeter for both static and dynamic power measurement.

For functional and most performance testing, input vectors will be loaded in the pattern generator and applied to the chip. Outputs of the SRAM will be sampled by the logic analyzer for functional verification and for coarse timing measurements. Precise timing measurements will be obtained using the sampling oscilloscope.

Static and dynamic power supply currents will be measured using the Keithley SourceMeter. This low noise meter makes it possible to measure leakage currents as smaller than 1 femtoamp, far below what is required for this application.

Tests to be performed include:

1. Functional. Use some benchmark input patterns at low speed to verify correct operation of both SRAM cores.
2. Performance and Dynamic Power. Use benchmark input patterns at high speed (up to the maximum for the logic analyzer) and observe outputs timing performance. At the same time, monitor supply current and voltage in order to determine dynamic power consumption.
3. Maximum Performance. Use the 1.1GBs data generator to determine the upper limit of the SRAM performance. Note: only very short, simple input vector sequences are possible. Outputs must be observed on the oscilloscope.
4. Static Power. Apply benchmark vector sequences slowly enough to allow transients to settle for each vector. Measure static current for each vector and collect statistics.
5. Gated-Ground Transistor Sizing Trade-Offs. Groups of ground rail gating transistors will variously be turned on (Vgs = Vdd), off (Vgs = 0), or strongly negatively biased (Vgs < 0) to approximate the effect of changing ground gate transistor width. Under conditions of differing effective transistor width, performance and power measurements will be repeated.

Results from each of these tests will be compared to the corresponding HSPICE simulation results.

**Reporting Plan**

Once the chip has been fabricated and tested, a report will be submitted to MOSIS which will include the following information:

1. Schematics and an explanation of the design.
2. HSPICE simulation results for performance, dynamic power, and static power, for a range of gated-ground transistor sizes.
3. Results from each of the tests described in the test plan.
4. A comparison and analysis of differences between HSPICE results and physical tests.
5. Conclusions and recommendations regarding the gated-ground technique, sizing of the gating transistors, and the accuracy and relevance of simulated circuit performance.

**Project Participants**

The chip was designed and will be tested by Hai Li and Amit Agrawal. Hai Li is a Ph.D. student studying VLSI circuit design and computer architecture in the School of Electrical and Computer Engineering at Purdue University. She received her M.S. and B.S. in Microelectronics at Tsinghua University. Amit Agrawal is an M.S.E.E. student in the School of Electrical and Computer Engineering of Purdue University, specializing in VLSI circuit design and microelectronics. He received the B. Tech degree in Electrical Engineering at the Indian Institute of Technology, Kanpur, India.

The work of Ms. Li and Mr. Agrawal is supervised by Prof. Kaushik Roy of the School of Electrical and Computer Engineering at Purdue University. He is a 1990 Ph.D. graduate of the University of Illinois and has been a faculty member at Purdue University since 1993. Prof. Roy supervises a large research group specializing in low power VLSI design and design automation for VLSI. He is extensively published and much in demand as a speaker and consultant on VLSI design and design automation.

Assisting Ms. Li and Mr. Agrawal with design flow issues and the MOSIS submission process is Dr. Mark C. Johnson, a professional staff member in the School of Electrical and Computer Engineering at Purdue University. Dr. Johnson is a 1998 Ph.D. graduate of Purdue University in the area of design automation for low power VLSI. Dr. Johnson’s official responsibilities are in the area of laboratory and curriculum development, but he is also active in research and consulting in the area of CAD for VLSI.