MOSIS Education Program RESEARCH Account
Enrollment Form

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Testing and Simulation tools:
Mentor Graphics

Enclosures: Background and qualifications of professors
Background and Qualifications of Professors

Tina Hudson has been working with integrated circuits for over eleven years. She received her Ph.D. in Electrical Engineering from Georgia Institute of Technology in December, 2000, focusing her research on the development of an integrated circuit implementation of muscular contraction. She has designed, fabricated, and tested five chips through the MOSIS foundry using several different processes. Currently, Dr. Hudson is an assistant professor at Rose-Hulman Institute of Technology, teaching the three quarter VLSI sequence. This sequence includes both analog and digital design, with an emphasis on layout techniques and testing methodologies. She was the CO-PI for a CCLI grant funded by NSF entitled, “Undergraduate VLSI Curriculum and Laboratory Emphasizing Mixed-Signal Circuit Design.” Additionally, she has had the opportunity to work in Georgia Tech’s Microelectronics Research Facility and Cornell’s National Nanofabrication Facility during undergraduate research projects. Her most recent publications are listed below.


**Project Description**

The goal of this project is to develop a real-time implementation of the properties exhibited by skeletal muscle using integrated circuits. The skeletal muscles used in mammalian movement control demonstrate unique properties that are not evident in engineered mechanical actuators. They produce smooth, graded movements over a wide dynamic range of output forces and, although based upon a common architecture, are utilized for very different tasks, e.g., writing and running. These characteristics make skeletal muscle an attractive model for inspiring new mechanical actuators that can be easily integrated into more naturally moving prostheses and autonomous robotic systems.

We are proposing to implement a circuit based upon a previous design that has been fabricated on an AMI 1.2um process through the MOSIS foundry that implements the behavior of the fundamental contractile element found in muscle tissue: a sarcomere. This circuit received a differential input voltage ($V_{L+}$ and $V_{L-}$) representing the length of the sarcomere, converted the differential length into a single ended output voltage ($V_L$), and calculated the velocity of sarcomere contraction ($V_{vel}$), as shown in Figure 1. Additionally, $V_L$ was used to calculate an activation factor, $V_\alpha$, which embeds the nonlinear force-length relationship demonstrated in biological muscles. $V_\alpha$ and $V_{vel}$ control an array of spatially coupled leaky capacitors that encode the number of force-contributing elements (crossbridges) in the sarcomere. The array produces an output current, $I_{force}$, that represents the force of the sarcomere. The force characteristics are modified by several parameters that set (i) the value of a current sourced onto the capacitors in the array of spatial elements ($f$), (ii) the value of a current sinking off the capacitors ($g$), (iii) the coupling between the capacitors ($c$), which is also effected by the velocity, and (iv) the force current contribution of each capacitor ($w$). The results of this circuit have been published in the Proceedings of The International Symposium on Circuit and Systems, 2001.

This circuit produced excellent results, demonstrating many of the nonlinear force characteristics exhibited by muscle tissue. However, the single ended output voltages, $V_{vel}$ and $V_\alpha$, required a comparison to an external voltage to properly control the array of spatial elements. This resulted in mismatch among sarcomere circuits when placed in an array. Therefore, we propose an

![Figure 1: Block diagram of circuit fabricated on AMI 1.2um process.](image-url)
improved sarcomere circuit that uses differential circuits for all blocks leading into the array of spatial elements, as shown in Figure 2. The block that computes the single ended voltage has been removed and the differential length ($V_{L+}$ and $V_{L-}$) directly controls the velocity and force-length blocks, which have been modified to receive this differential input. Additionally, the force-length block has been modified to reflect a shift in the force-length relationship as a function of an input voltage representing neural stimulation rate ($V_{SR}$).

We are interested in implementing this project on the TSMC process for several reasons. By utilizing the submicron feature size, we may be able to create an array of these sarcomere circuits that interact with one another, mimicking a behavior that has been hypothesized to occur in muscle fibers by the neuroscience and physiology community. Before creating the array, we must first characterize a single sarcomere circuit. Additionally, the TSMC process exhibits excellent matching among transistors, which will aid in minimizing noise in our circuits operating in the subthreshold regime. Finally, this will be an excellent opportunity for one of our students, Christian Mboula, to obtain experience with a submicron process.

**Estimated Project Size**

We estimate that this project will require a 5mm X 5mm die bonded in a 40 pin DIP package on the TSMC 0.35um process. Five parts are sufficient to characterize the circuit and test for mismatch among chips.

**Simulation Plans**

We have already begun simulation of the modified blocks in the circuit. Using Accusim in the Mentor Graphic Design Kit, we have simulated the new force-length block (circuit shown in Figure 3a) and the velocity block (circuit shown in Figure 3b). We are using a BSIM model provided by Mentor Graphics in their ASIC Design Kit. We have characterized each block as a function of each of their parameters so that we know the best parameter space for proper circuit operation. These blocks have been laid out, extracted, and tested once again to verify the effects of stray capacitance and resistance. After integrating the new blocks with the previous layout, we will verify that the entire layout matches the expected design by using the Mentor Graphics LVS tool.
which verifies matching transistor sizes as well as basic circuit topology. Unfortunately, we are unable to simulate the layout of the entire chip because the large number of transistors operating in their analog regime. However, because the array of spatial elements block has been previously fabricated and the new circuit blocks have been thoroughly tested, we are confident that the entire circuit should operate as expected.

**Testing and Characterization Plans**

We will test this circuit using two DAC boards controlled by a pic controller to set the large number of parameters. A java applet will control the pic controller for easy modification of the parameters. The current output, $I_{\text{force}}$, will be converted into a voltage using a discrete op-amp with external resistors. This output voltage will be sent to a GPIB controlled oscilloscope. A computer will extract data from the oscilloscope and transfer it into MATLAB for observation and recording.

First, we will test the new blocks individually by measuring $V_{\text{vel}}$ and $V_\alpha$ as a function of the differential length. We will also test the input common mode range of these circuits so that we will know the range of inputs that can be placed across a series array of sarcomere circuits.

Next, we will see how these circuits operate in the whole system by repeating these tests and measuring $I_{\text{force}}$. A multiplexer allows either $V_\alpha$ or an external voltage to control the force-length block so that we can separate the effects of the velocity block and the length block on $I_{\text{force}}$. Then, we will measure the effects of both of these blocks on $I_{\text{force}}$. 

Figure 3: (a) Circuit contained in force-length block. (b) Circuit contained in velocity block.
We will also evaluate the mismatch in the circuit by measuring and comparing the output voltages on the capacitors in the array of spatial elements. Capacitor voltages can be compared to other capacitors on the same chip and between different chips.