Design | Fab ID | Design Name | Technology | Size mm$^2$
--- | --- | --- | --- | ---
63096 | T18JAE | driver_vod_20010 | TSMC35_P2_NEW | 4.61

**Designer:** Guangbin Zhang, Ph.D. student in EE department of UTDallas

**Faculty advisor:** Dr. Jin Liu

**Test Report:**

This project is a design of an accurate CMOS current source for low voltage current-mode transmitter drivers. It is composed of binary weighted current mirrors and built-in-self-test structures for self-measurement and calibration. The first chip of this design has been fabricated through as project 63096.

Test results show that the scheme of the self-calibration works very well. Fig. 1 shows that the output of the binary weighted current mode driver has good linearity. Fig. 2 shows the driver’s output accuracy with or without the self-calibration (test result). The switches $Q_x$ automatically turned on or off while the reference voltage of current mode driver changes. Without the self-calibration, the output varies more than $\pm 7\%$ while driver’s current reference varies, while it only varies $\pm 1\%$ with the self-calibration (an external switch is used to set the self-calibration circuit on or off in this trial chip).

![Graph showing output linearity](image_url)

**Fig. 1.** The output of the binary weighted current mode driver with manual adjust
However, the accuracy of the first chip is not as good as we expected. We did some testing and analyzing and found several problems of this chip. The error mainly comes from the resistor mismatch and comparator input offset in the self-calibration loop.

First is the resistor mismatch of the opamp subtracter. The ratio of the resistor change from 4:1 to 5.3:1. We used 5 identical layout poly2 resistors to realize the 4:1 ratio, however, seems other factors, such as the interconnection, position, dummy layouts, and the substrate contact also contribute a lot to the total ratio. We should consider about these factors more carefully later.

Second is the offset and the gain of the comparator. We use the CMC cmosp35.3.0 design kit for simulation. It shows the comparator gain is about 7000. However, the tested gain of the real chip is only about 300. We did the simulation again with the models from MOSIS for this run (T18JAE), found that the gain is about 450, which is near the tested result. We guess that the model parameters in CMC kit is not updated enough to fit for the recent fabrication. Anyway, we should re-design the comparator to get high gain.

The offsets of the comparators are much higher than we expected. The maximum offset caused by process variation we’ve found is 55mv, while we expect it smaller than 10mv.

We propose to use the following methods to solve them and improve the accuracy in future design.

1. To improve the matching of the resistors used in a subtracter.
   Solution:
   a. Use dummy resistors and the end of the resistor array
   b. Use centroidal symmetry layout
   c. Use more tank contact to minimize the substrate current effect
   d. Avoid metal lead goes above the resistors

2. To reduce the comparator offsets and enlarge its gain.
   Solution:
a. Use positive feedback to improve the gain of the comparators
b. Use auto-zero circuits to minimize the offsets of the comparators
c. Use larger MOSFET size to reduce the mismatch

3. The performance of the opamp seems being affected by the main driver’s large output current.
   Solution:
   Add enough space and substrate contact between the main driver and other parts of the circuitry.

4. One narrow pulse (2ns) in digital logic circuit is filtered out by the parasitic capacitor introduced by the wide wire to the pad.
   Solution:
   Revise the digital logic to avoid this kind of ultra-fast pulses

5. On-chip complementary signal generator needs to be built. It’s impossible to achieve good high frequency complementary signals off-chip.
Appendix. Original proposal for project 63096:

Proposal for MEP research account
Title: Self-calibrated Transmitter Driver (TSMC35_P2)

Project Description:
This project is a design of an accurate CMOS current source for low voltage current-mode transmitter drivers. It is composed of binary weighted current mirrors and built-in-self-test structures for self-measurement and calibration.

To achieve long transmission distance without causing strong emission, current mode transmitter drivers require accurate current sources, which are usually implemented by cascode current mirrors. But, due to the limited signal swing range in low voltage supply applications, the cascode method cannot be used. Different techniques have been developed to improve the accuracy of current mirrors in low voltage supply applications. The main principle used by these techniques is to match the drain-source voltages of the mirroring transistors, even when the transistors operate in the non-saturated region. For example, operational amplifiers (opamp) have been used to match the drain voltages of the mirroring transistors. However, there are many other factors that can cause the current source to be inaccurate, such as process variation, temperature variation, voltage supply variation, and the aging of components. To compensate for these factors, tunable current mirrors have been developed. The binary weighted digital tunable CMOS current mirror proposed in is a generic tunable current mirror architecture, which can be tuned by different kinds of trimming or tuning methods without re-fabrication. However, the manufacturing cost of currently available trimming methods is usually prohibitive.

Proposed in this project is an on-chip self-measurement and self-calibration scheme to automatically measure and tune the binary weighted current mirrors, so that the output current is within a range around the desired value. The manufacturing cost of the on-chip self-calibration circuits is minimal, compared with the currently available trimming methods.

The basic idea of this design is to use a binary-weighted current mirror. The current is mirrored from a current reference to five pairs of simple current sources (sinks). One of them is the main mirror. The other four are binary weighted with relative size of 1x, 2x, 4x, and 8x. The main mirror is always on. The other four can be turned on or turned off by the switches, controlled by the binary code \( Q_0, Q_1, Q_2, \) and \( Q_3 \). The total output current, \( i_{\text{out}} \), can be expressed by the
following equation: $i_{out} = i_{main} + Q_0i_0 + Q_1i_1 + Q_2i_2 + Q_3i_3$, where $i_{main}$ is the current of the main current source (sink), $i_0$, $i_1$, $i_2$, and $i_3$ are the currents of the current sources (sinks) with size of 1x, 2x, 4x, and 8x respectively, and $Q_0$, $Q_1$, $Q_2$, $Q_3$ are the binary codes that control the switches of the binary weighted current sources (sinks).

The output of the current-mode driver is the driver output voltage, $v_{out}$, which is determined by $v_{out} = i_{out}R_L$, where $i_{out}$ the total output current and $R_L$ is the external resistance.

Then we use a self-calibration circuit to adjust the current source automatically, the first step is to measure the value of the current. The value measured is the output voltage, $v_{out}$. In order to achieve maximum measurement accuracy, source followers are used as buffers between the driver and the measurement circuit. After the source followers, the differential signal is transferred to single-ended signal by a subtracter, composed of a high gain opamp and several resistors.

Then, the single-ended output voltage is compared with the desired reference voltage, $V_{REF}$, by a pair of comparators. In the proposed design, we use the offset voltage of comparators to define a range. If the offset voltage of the comparator is $V_{OS}$, the range will be $V_{REF} \pm V_{OS}$. If the output voltage is within this range, the following counter will not be triggered, thus the output binary bits remain the same. If the output voltage is outside this range, the counter will either count up or count down one bit every clock cycle and the binary bits will change accordingly.

The next stage of the self-calibration circuit is a counter. Since the main current source usually provides less current than desired, the counter will usually count up; to selectively turn on some of the binary weighted current sources. After the current reach the desired range, the counter will stop counting up. If, the output current is higher than the desired current, the counter will count down and again stop counting when the current is within the defined range. In order to make the measurement of the driver’s output easier for high-frequency application, a dummy circuit that runs in constant signal input is used.

**Estimated Project Size and Simulation Plans:**
The circuit has been simulated by Cadence Analog Artist with SpectreS. The layout has been done using TSMC35_P2_NEW process. The total area is 2149µm x 2149 µm. Simulation
results show that this design can compensate the variations of process, temperature, and voltage supply to get higher current precision.

**Test and Characterization Plans:**

After the fabrication of the chip, we are going to carry out a serial of tests. The inputs of the chip are 3.3v voltage supply, several reference voltages, and several external digital control signals. We are going to vary the voltage supply and reference voltages and other conditions to test the accuracy and durable range of this driver. Some important internal points of the circuit have been linked out to the pins so that we can measure those voltages during the chip testing. Several pins have been multi-used to add more testing signals into the chip. The chip will be tested in the Analog and Mixed Signal IC Design and Test Lab in the University of Texas at Dallas. Available equipments are GHz range oscilloscopes, SMUs, power supplies, etc.

If possible, we would like to send out this design for fabrication on the TSMC_2P process dated Aug. 13, 2001.

**Contact:**

Jin Liu Ph.D.
Assistant Professor
Analog Integrated Circuit Design
Department of Electrical Engineering
Erik Jonsson School of Eng. and CS.
University of Texas at Dallas
P.O. Box 830688, EC33
Richardson, TX 75083-0688
Office: EC 2.506
Phone: (972) 883-4393
Fax: (972) 883-2710
Email: jinliu@utdallas.edu
Web: www.utdallas.edu/~jinliu